AXIe-1: Base Architecture Specification

Revision 3.1

January 11, 2018

Important Information

AXIe-1 Base Architecture Specification is authored by the AXIe Consortium companies. For a vendor membership roster list, please contact execdir@axiestandard.org.

The AXIe Consortium wants to receive your comments on this specification. To provide such feedback, or to join the consortium, contact execdir@axiestandard.org.

Warranty

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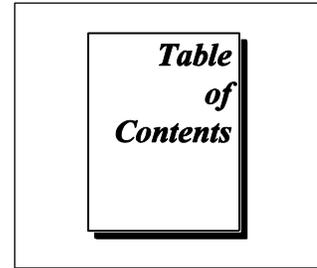
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AXIe-1 Base Architecture Specification

Revision History

This section is an overview of the revision history of the AXIe-1 specification.

Table 1-1. Architecture Specification Revisions

Revision Number	Date of Revision	Revision Notes
1.0	June 30, 2010	Initial Version
2.0	September 5, 2013	Deleted Instrument Hub slot and module specifications, making logical slot 2 an ordinary instrument slot. Added platform management requirements for multiple-slot modules. Added power-up and power-down sequencing requirements to better support CPU modules and PCIe enumeration. Updated Figure 6-1 and Table 6-5 with the correct local bus channel pair numbering. Moved the fabric channel coupling capacitors to the transmit end of the channels. Clarified the local bus electrical and e-keying requirements. Added CLK100 feedback pair to the system slot. Clarified trigger bus driver and receiver requirements.
3.0	October 8, 2015	Added support of 8 and 16 lane PCI Express® links to instruments in integrated chassis. Added prrovision to accommodate AXIe-0 unmanaged modules. Cleaned up typos and formatting errors.
3.1	Jan 11, 2018	Removed sections 8 and 9 which were related to compliance and incorporated them into AXIe-Compliance Requirements and Trademarks usage document.

1. Overview of the AXIe Base Specification

1.1 AXIe Compliance

This specification is for use with other AXIe specifications. The AXIe consortium places limitations on the use of the AXIe trademark and requires compliance with certain companion standards. Detailed compliance requirements and trademark usage requirements are in the AXIe Compliance Requirements and Trademark Usage document.

1.2 Introduction

The AXIe Base Architecture defines an extensible platform for general purpose, modular instrumentation. The architecture incorporates the best features of earlier modular open instrumentation platforms, including VXIbus, PXI, and LXI. Like VXIbus and PXI, the architecture is based on a popular modular computing platform with added features important to developers and users of test and measurement systems. The base platform is AdvancedTCA®, an open architecture for modular computing components targeted for communications infrastructure applications. The AdvancedTCA® architecture includes provisions for power distribution, power and system management, Ethernet communication between modules, and PCI Express® communication between modules, along with other capabilities. The AXIe Base Architecture includes some modifications to the AdvancedTCA® architecture. These modifications provide timing, triggering, and module-to-module data movement features that are important to the implementation of high-performance test and measurement systems.

AXIe, like other modular instrumentation platform specifications, defines a set of mechanical, electrical, and logical interfaces between instrumentation *modules* and *chassis*. A typical AXIe chassis and module are illustrated in Figure 1-1, and a simplified chassis block diagram is shown in Figure 1-2. AXIe modules slide into slots in the chassis' front subrack, and engage connectors on the backplane. The backplane provides power and system management connections to the modules, and control, data, trigger, and timing connections between the modules. The shelf manager is a dedicated system management controller that monitors the health of the chassis subsystems and modules, controls the chassis cooling fans, and manages the chassis power-up sequence. The modules house various functions related to the test/measurement application, including (but not limited to) signal measurement, signal sources, digital IO, data communication, signal analysis, and general purpose computing. All external IO in an AXIe-1 system is through connectors on the front faceplates of the AXIe modules.
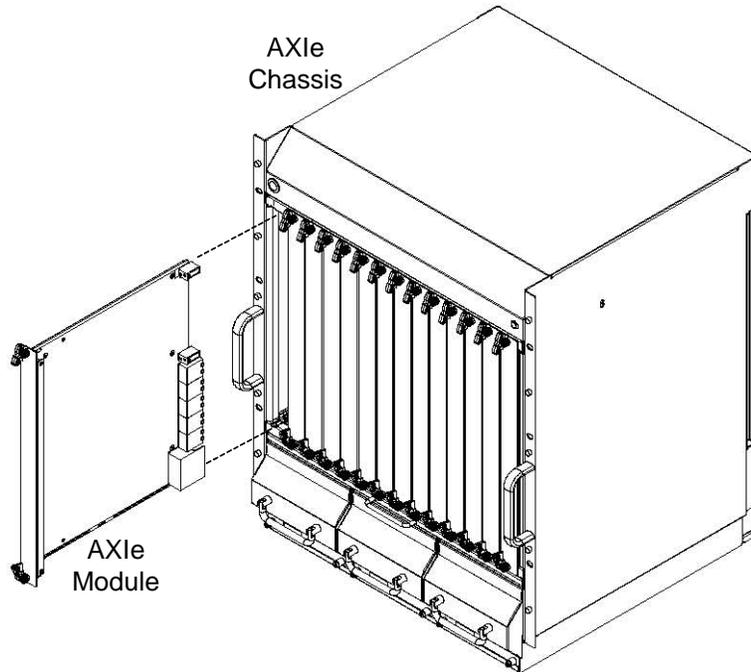
Figure 1-1: AXIe chassis and module.

The AXIe backplane supports two serial interface standards, LAN and PCI Express®. Both interfaces are suitable for module control and measurement data transfer. Most AXIe modules support one or the other of these interfaces. A few modules may connect to both interfaces. The LAN interface is best suited to intelligent modules that support high-level command interfaces. These LAN connected AXIe modules are expected to conform to many of the LXI protocols and usability requirements as specified by the AXIe-2 Software Specification. The PCI Express® interface is best suited for less intelligent modules that require low-level register control. These PCI Express® modules operate as extensions of the host computer and appear to the host operating system as standard PCI Express® peripherals. In addition, these modules are required to conform to most of the PXI software requirements, as defined by the AXIe-2 Software Specification. Thus the integration, programming, and use models of both types of modules are already familiar to most test system integrators and users.

Chassis Rear
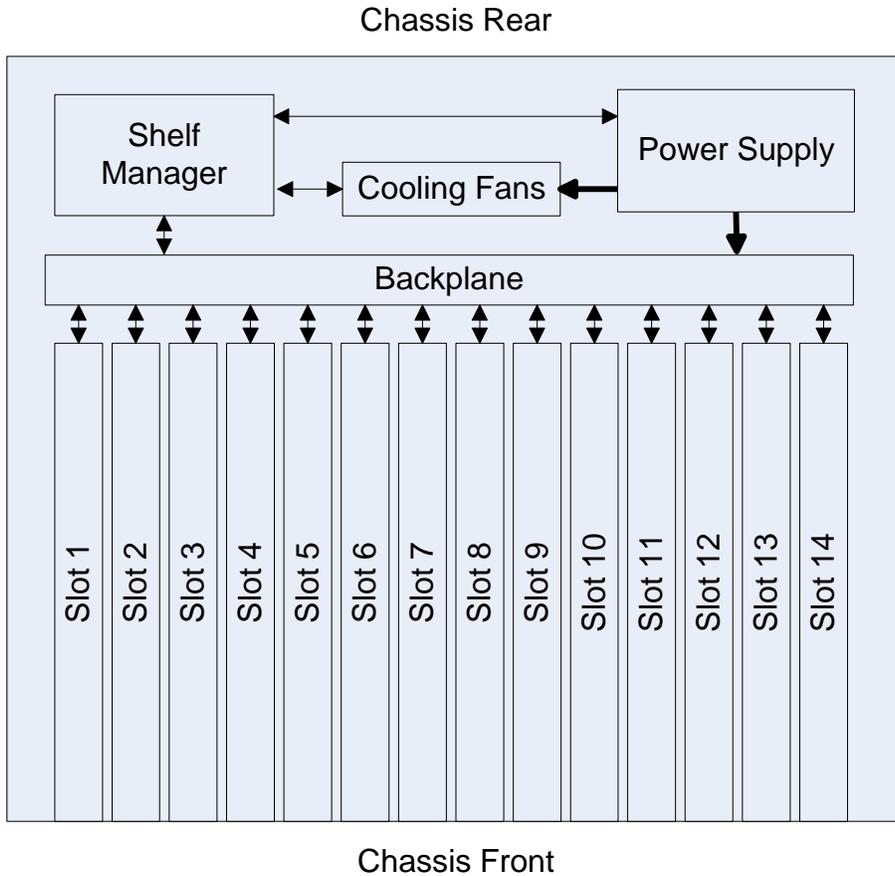
Figure 1-2: AXIe chassis block diagram.

AXIe modules are ~320 mm tall, ~280 mm deep, and ~30 mm wide. They each typically dissipate 100 - 200 W of power. The large board area, module volume, and high power capability make the AXIe platform especially well suited for applications that require large channel counts, high performance measurements, and/or efficient use of rack space.

The AXIe-1 specification defines a general-purpose test and measurement platform. Related AXIe-3.n specifications may define extensions to the AXIe-1 architecture optimized for particular market segments. The AXIe-3.1 specification defines extensions optimized for semiconductor test systems.

1.3 Audience of Specification

This specification is primarily for the use of AXIe equipment manufacturers and system integrators who are implementing products and systems that conform to the requirements of this specification. The primary audience is assumed to have extensive knowledge of modular measurement hardware architectures, and access to the various referenced technical specifications. However, this specification should also prove useful to managers and anyone else involved in the selection of modular test system platforms and architectures.

1.4 Organization of Specification

This specification consists of a system of numbered RULES, RECOMMENDATIONS, PERMISSIONS, and OBSERVATIONS, along with supporting text, tables, and figures.

RULEs outline the core requirements of the specification. They are characterized by the keyword "**SHALL**". Conformance to these rules provides the necessary level of compatibility to support the multi-vendor interoperability expected by system integrators and end users in the test and measurement industry. Products that conform to this specification must meet all of the requirements spelled out in the various rules.

RECOMMENDATIONs provide additional guidance that will help AXIe equipment manufacturers improve their users' experiences with AXIe systems. They are characterized by the keyword "**SHOULD**". Following the recommendations should improve the functionality, flexibility, interoperability, and/or usability of AXIe products. Products are not required to implement the recommendations.

PERMISSIONs explicitly highlight some of the flexibility of the AXIe specification. They are characterized by the keyword "**MAY**". The permissions generally clarify the range of design choices that are available to product and system designers at their discretion. They allow designers to trade off functionality, cost, and other factors in order to produce products that meet their users' expectations. Permissions are neutral and imply no preference as to their implementation.

OBSERVATIONs explicitly highlight some of the important nuances of the specification. They help the readers to fully understand some of the implications of the specification's requirements and/or the rationale behind particular requirements. They generally provide valuable design guidance.

All rules, recommendations, permissions, and observations must be considered in the context of the surrounding text, tables, and figures. Rules may explicitly or implicitly incorporate information from the text, tables, and figures. Although the authors of this specification have gone to significant effort to insure that all of the necessary requirements are spelled out in the rules, it is possible that some important requirements appear only in the specification's free text. Conservative design practice dictates that such embedded requirements be treated as rules.

The AXIe-1 specification is based on the AdvancedTCA® specification. The relevant AdvancedTCA® numbered requirements are explicitly referenced in this specification's rules, recommendations, permissions, and observations. These requirements are incorporated along with their supporting context (text, tables, figures, etc.). Any AdvancedTCA® numbered requirement that is not explicitly included by this specification's rules, recommendations, permissions, or observations, is excluded from the AXIe-1 requirements.

Successful implementation of AXIe products and systems requires in-depth knowledge of this AXIe-1 specification and the AdvancedTCA® specification. This specification does not reproduce any content from the AdvancedTCA® specification, beyond the high-level description in Section 1.5.1.1"AdvancedTCA® Overview".

1.5 Architecture Overview

The AXIe architecture consists of hardware and software requirements that support the smooth multi-vendor integration of AXIe modules and chassis into powerful test systems. The architectural foundation of AXIe is the AdvancedTCA® specification which defines a modular platform optimized for telecom central office applications. AXIe adds several hardware and software features that are important to the test and measurement marketplace.

1.5.1 AdvancedTCA® Features

The AXIe architecture is based largely on the AdvancedTCA® architecture and incorporates many of its features. The following sections provide a brief overview of the AdvancedTCA® architecture and a summary of the features that the AXIe architecture includes and excludes.

1.5.1.1 AdvancedTCA® Overview

The AdvancedTCA® specification defines an open architecture for modular computing components for high-availability network and telecom service installations. The basic mechanical elements are front boards, rear transition modules (RTMs), backplanes, and subracks. The front boards provide the core system functionality, while the RTMs provide user-defined external IO connections through the rear of the system. The backplane provides connector interfaces for both front board IO and power distribution, while the subrack provides the mechanical support of the

front boards and RTMs.   A single backplane and subrack may support up to 16 front boards (and matching RTMs). Figure 1-3 illustrates the physical relationships between front boards, backplanes, and RTMs.
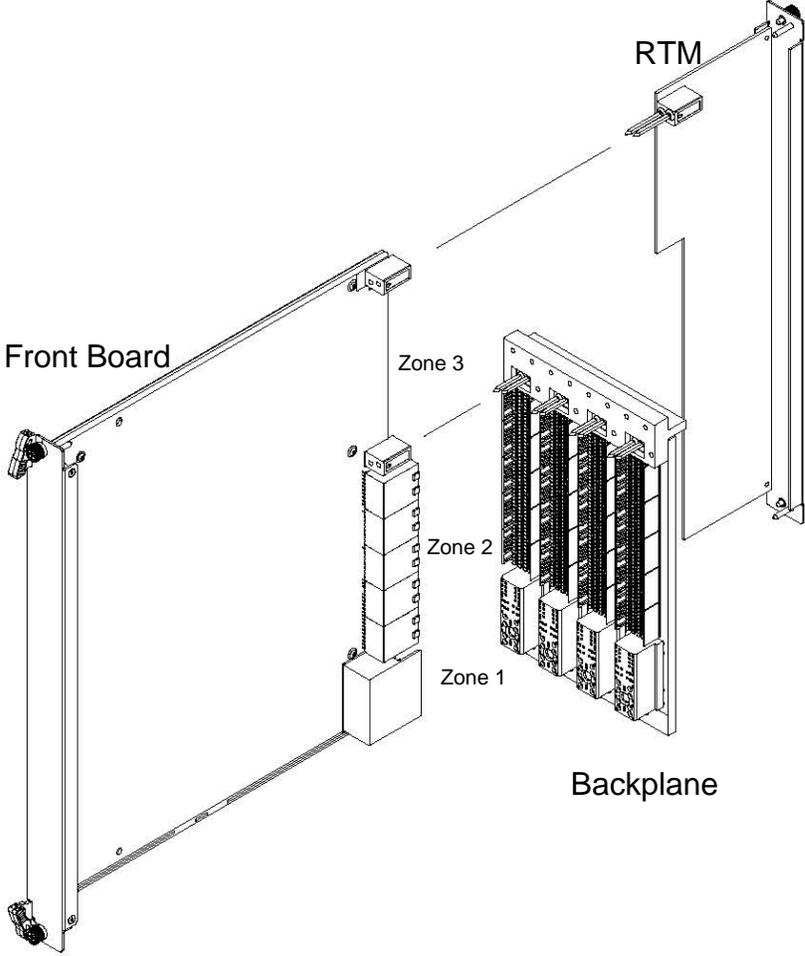
Figure 1-3: AdvancedTCA® front board, backplane, and RTM.

The front board, shown in Figure 1-4, is 322.75 mm tall, 30.48 mm wide, and about 280 mm deep. It includes a front face plate with injector/ejector handles. The backplane connector region is divided into 3 zones. Zone 1 includes power and platform management signals. Zone 2 includes data transport signals, and Zone 3 includes IO signals to the RTM.

Figure 1-4: AdvancedTCA® front board.

AdvancedTCA® includes an extensive platform management system that includes a central shelf manager and distributed management controllers. The system monitors the health of the system, manages the system power and cooling, and oversees the compatibility of the module interconnects. The AdvancedTCA® architecture is designed for 99.999% availability, supported by dual redundancy of critical resources, board hot swap, etc.

Systems are designed to operate from -48 VDC battery power, which is commonly available in telecom central offices. This power is distributed directly to the front boards, using redundant power feeds.

AdvancedTCA® includes extensive cooling characterization requirements that enable system integrators to assemble systems in which all components receive adequate cooling.

The zone 2 interconnect includes various interfaces for module-to-module communication. There is a base interface for LAN signaling that is connected in a dual-redundant star topology. There is a similar fabric interface that can be used for a variety of signaling schemes, including PCI Express®. It is usually connected in a dual-star topology. Two of the front boards serve as hubs for the base and fabric stars, providing the switching resources necessary for the operation of the base and fabric interfaces. The fabric interface may support other topologies, including a full mesh. There is also a synchronization clock interface, which provides bused telecom clocks across the backplane, and an update channel interface which provides for proprietary communication between compatible boards. All signal connections in zone 2 are differential pairs.

1.5.1.2 AdvancedTCA® Features Included in AXIe

The following sections provide a summary of the AdvancedTCA® features that are also part of the AXIe architecture.

1.5.1.2.1 Mechanical

The AXIe architecture incorporates all of the AdvancedTCA® mechanical requirements for front board assemblies, Zone 1 and Zone 2 backplane connectors, backplanes, and subracks, with only a few exceptions related to the required number of slots, and support of rear transition modules, and environmental requirements. Unlike AdvancedTCA®, AXIe systems are often used in laboratory and production environments. These environments are typically different than the central office equipment room environments where AdvancedTCA® equipment is usually deployed. These differences may include power delivery systems, ambient temperature range, acoustic limits, EMC, etc. In general, each AXIe equipment manufacturer is responsible for determining and specifying the suitable environmental requirements for its AXIe products.

1.5.1.2.2 Hardware Platform Management

The AXIe architecture incorporates most of the hardware platform management features of AdvancedTCA® and requires AXIe devices and system components to comply with all applicable AdvancedTCA® hardware platform management requirements, with a few exceptions related to redundancy and telecom-specific functions. The AXIe architecture also incorporates some extensions to the electronic keying scheme in order to support unique AXIe features and requirements.

1.5.1.2.3 Power Distribution

The AXIe architecture incorporates the AdvancedTCA® power-distribution scheme for backplanes and front boards, with exceptions related to redundancy and the distributed voltage tolerance range. Advanced TCA® is targeted for applications that are powered from external 48V battery plants. AXIe products are typically used in locations where the primary power source is the local AC power mains. Thus a typical AXIe chassis will include a power supply unit (PSU) that converts a range of AC line voltages/frequencies to the 48VDC distributed on the AXIe backplane.

1.5.1.2.4 Thermal

The AXIe architecture incorporates the AdvancedTCA® thermal requirements for front boards and shelf front board slots. Typical AXIe applications don't require the cooling system redundancy that is expected in most Advanced TCA applications.

1.5.1.2.5 Data Transport

The AXIe architecture incorporates the AdvancedTCA® requirements for Zone 2 base and fabric interfaces for backplanes and front boards, with exceptions related to redundancy. AXIe systems are limited to a single-star topology for the base interface (LAN) and a single-star topology for the fabric interface.

1.5.1.2.6 PICMG® 3.4 PCI Express® Fabric

The AXIe architecture incorporates the requirements for the PCI Express® fabric interface as defined in the PICMG® 3.4 extension to the AdvancedTCA® specification. The architecture supports up to 16 PCI Express® lanes to each instrument module.

1.5.1.3 Differences from AdvancedTCA®

The following sections provide a summary of the AdvancedTCA® features that are excluded from the AXIe architecture.

1.5.1.3.1 No Requirements for Redundancy

The general-purpose test and measurement marketplace does not have the 99.999% availability requirement expected in the telecom marketplace. Thus the AXIe architecture does not require use of the redundancy features specified in AdvancedTCA®. Modules and systems may optionally implement the redundant power distribution scheme. Use of the redundant power management bus is not required. The Hub 2 base and fabric channels are not routed on AXIe backplanes.

1.5.1.3.2 No Rear Transition Modules

AXIe-1 systems do not use rear transition modules. Measurement I/O signals are routed through the front modules' faceplates. Mainframes are not required to provide rear transition module slots. Subsequent AXIe-3.n specifications may define Zone 3 backplane or rear transition module schemes for particular markets. The AXIe-1 module envelopes are defined to prevent AXIe-1 modules from interfering with AXIe-3.n zone 3 backplane connectors that fit within a defined envelope.

1.5.1.3.3 Maximum of 14 Slots

General-purpose instrumentation equipment is typically designed for mounting in 19" EIA racks. This allows room for only 14 vertical slots. The AXIe-1 architecture permits a maximum of 14 slots in a mainframe, instead of the 16 slots allowed in AdvancedTCA® shelves.

1.5.1.3.4 No External Shelf Mechanical, Electrical, or Environmental Requirements

The AXIe architecture is focused on compatibility between modules, backplanes, subracks, and other system components within a chassis. The power source, dimensions, environmental specifications, and regulatory requirements are determined by each AXIe chassis supplier according to market needs.

1.5.1.3.5 Modified Synchronization Clock Interface

The AXIe architecture expands the use of the Synchronization Clock Interface for additional purposes beyond those defined in AdvancedTCA®. AXIe backplanes maintain the bused topology of most of the Synchronization Clock signals, and devices implement the same MLVDS signaling levels as AdvancedTCA®. However, the bus is used for general-purpose synchronization and triggering by AXIe modules, and AXIe systems do not generally distribute the specific clock signals defined by AdvancedTCA® (although such use is permissible within the AXIe architecture).

1.5.1.3.6 No Update Channel Interface

The AXIe architecture does not implement the Update Channel Interface as it is defined in AdvancedTCA®, which allows a variety of backplane topologies and implementations. AXIe backplanes implement a single bused MLVDS topology for the signals connecting to those Zone 2 connector contacts, and devices implement different signaling schemes as defined in this specification. AXIe devices and system components implement electronic keying appropriate to prevent incompatible connections between AXIe and AdvancedTCA® devices installed in either system environment.

1.5.2 AXIe Extensions to AdvancedTCA®

The AXIe architecture provides several features not found in AdvancedTCA®. It also places additional restrictions on modules and system components in order to assure a higher level of interoperability. The following sections summarize these features and restrictions.

1.5.2.1 AXIe Trigger Bus

One obvious differentiating feature is the AXIe Trigger Bus, TRIG[0-11], which consists of 12 MLVDS trigger pairs bused across all of the slots on an AXIe backplane. This bus (together with the AXIe Timing Interface and Local Bus) is implemented using the Zone 2 connector contact positions that are used for the Update Channel, Synchronization Clock, and Slot 15 and 16 fabric channels in AdvancedTCA®.

1.5.2.2 AXIe Timing Interface

Another obvious differentiating feature is the AXIe Timing Interface, which includes star clock (CLK100), star synchronization (SYNC), star trigger (STRIG), and fabric clock (FCLK) signals. This interface is implemented using some of the Zone 2 connector contact positions that are used for the Update Channel, Synchronization Clock, and Slot 15 and 16 Data fabric channels in AdvancedTCA®. The timing interface topology is shown in Figure 1-5.
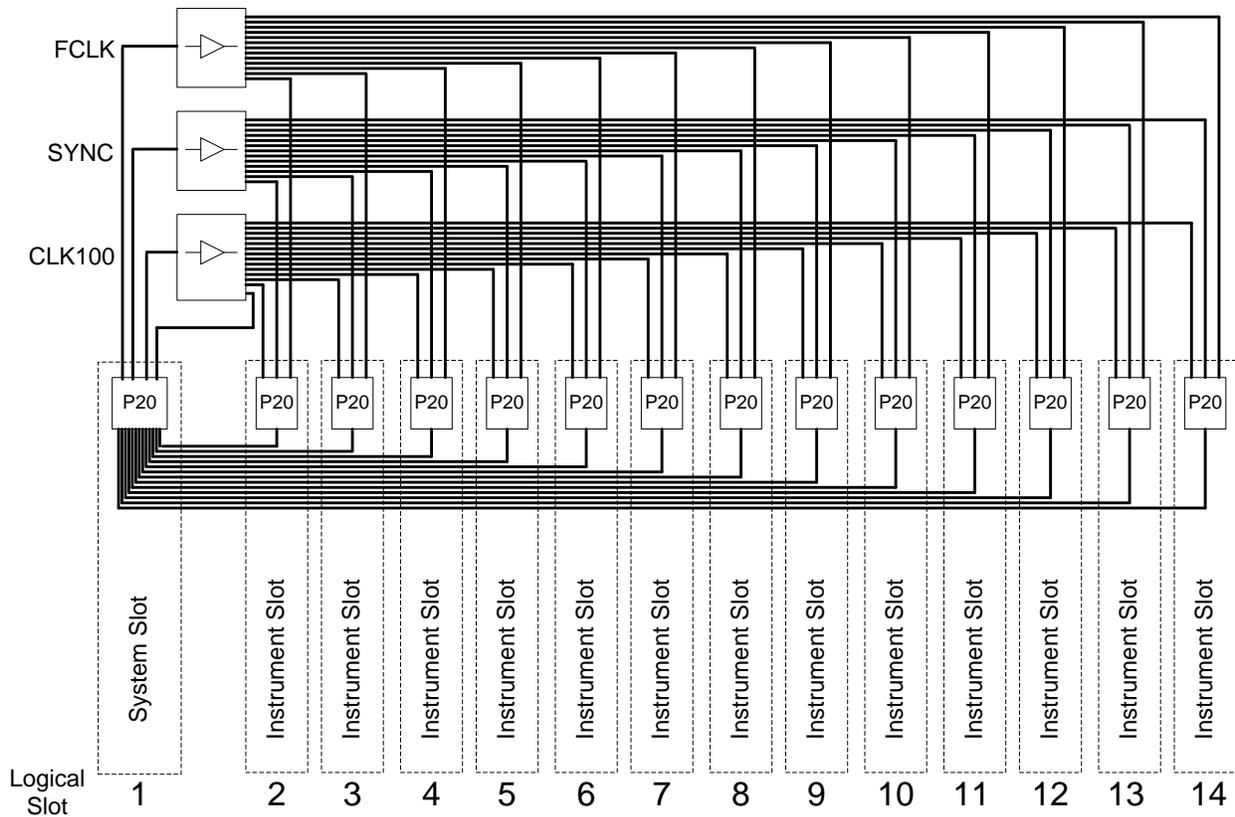
Figure 1-5: AXI timing interface.

1.5.2.2.1 CLK100, SYNC, and STRIG Pairs

The CLK100 backplane star distributes a differential 100 MHZ clock from the system slot to the instrument slots. The SYNC star distributes a differential trigger signal from the system slot to the instrument slots. Both the CLK100 and SYNC fabrics have active drivers to fan-out the signals, which are each sourced from the system slot using a single pair. The STRIG star carries bi-directional trigger signals between the system slot and the instrument slots. Each unbuffered Star Trigger signal terminates at the system slot on its own connector pair.

1.5.2.2.2 FCLK (PCI Express® Reference Clock Distribution)

AXIe backplanes provide for distribution of a 100 MHz PCI Express® reference clock, FCLK, from the system slot to all of the other slots. The FCLK fabric includes active buffers to fan-out the clock as individual, point-to-point differential pairs.

1.5.2.3 AXIe Local Bus

The AXIe local bus provides short differential signal pairs between adjacent AXIe slots, excluding the system slot. There are 18 required local bus pairs in each slot-to-slot segment. Backplanes may optionally provide local bus expansion to 42 or 62 pairs.

1.5.2.4 Future Zone 3 Extensions

The AXIe architecture is intended to be extensible beyond the needs of general-purpose test and measurement equipment. Future supplemental AXIe specifications (AXIe-3.1, AXIe-3.2, etc.) may add additional features and configurations. These are likely to include the definition of one or more Zone 3 backplane connector configurations.

1.5.2.5 No Hub 2 Use

Because AXIe does not require the redundancy features of AdvancedTCA®, the Hub 2 (logical slot 2) base and fabric channels are not used in AXIe. AXIe systems do not support AdvancedTCA® Hub devices in logical slot 2. Instead, logical slot 2 is defined as an ordinary instrument slot.

1.5.2.6 Additional Electronic Keying

The AXIe architecture requires that devices and systems implement an extended set of electronic keying records to assure the consistent use of AXIe-defined backplane fabrics and resources.

1.5.2.7 Additional System Management Requirements

The AXIe architecture requires that each chassis include a dedicated shelf manager.

1.5.2.8 Internal EMC Requirements

The AXIe architecture includes EMC requirements for modules and system components that should prevent measurement integrity problems due to electromagnetic interference from components within an AXIe mainframe.

1.6 References

Several other documents and specifications are related to this specification. These include:

- PICMG® 3.0 Revision 3.0, AdvancedTCA® Base Specification, PCI Industrial Computer Manufacturers Group (PICMG®), 401 Edgewater Place, Suite 600, Wakefield, MA 01880 USA, Tel: 781.246.9318, Fax: 781.224.1239, www.picmg.org.
- PICMG® 3.4 Revision 1.0, PCI Express®/Advanced Switching for AdvancedTCA® Systems, PCI Industrial Computer Manufacturers Group (PICMG®).
- PCI Express® Base Specification, Revision 2.1, PCI-SIG®, www.pcisig.com.
- PCI Express® Card Electromechanical Specification, Revision 2.0, PCI-SIG®.
- VXI-1 Revision 3.0, VMEbus Extensions for Instrumentation System Specification, VXIbus Consortium, www.vxibus.org.
- PXI-5 Revision 1.0, PXI Express Hardware Specification, PXI System Alliance, www.pxisa.org.
- LXI Standard Revision 1.3, LAN Extensions for Instrumentation, LXI Consortium, www.lxistandard.org.

1.7 Terminology

AXIe terminology is modeled largely on language familiar to manufacturers, system integrators, and end users in the test and measurement industry. In many cases this is different from the telecom-derived terminology used in the AdvancedTCA® specification.

1.7.1 AXIe Terms

Here are the definitions of some of the more common AXIe terms:

- *Chassis -* This is the primary AXIe infrastructure component that hosts AXIe modules. A typical AXIe chassis includes a backplane, subrack, power supply(ies), fan tray(s), shelf manager, and sheet metal enclosure. It may include rack mounting provisions. A chassis may also include an *embedded system module.* (See *Integrated Chassis.)*
- *Integrated Chassis -* An AXIe chassis that has built-in system module functionality in lieu of an AXIe-standard system slot.
- *Module -* A PC assembly, face plate, and enclosure that plugs into an AXIe slot. Equivalent to an AdvancedTCA® *front board.*

- **System Module -** An AXIe module that includes LAN switches, PCIe® switches, system timing and trigger resources, and/or other central resources. A system module installs in a chassis system slot. An AXIe system module is comparable to an AdvancedTCA® *hub board.*
- **Embedded System Module -** System module functionality that is embedded in an *integrated chassis.*
- **System Slot -** An AXIe slot that supports a *system module.* It is always *logical slot 1.* It is comparable to an AdvancedTCA® *hub slot.*
- **Instrument Module -** Any AXIe module that is not a *system module.*
- **AXIe Timing Interface -** A collection of star-topology signal pairs that carry AXIe timing signals between the *system slot* and the *instrument slots.* The timing signals are CLK100, SYNC, STRIG, and FCLK.
- **AXIe Trigger Bus -** A set of 12 MLVDS signal pairs, TRIG(0:11), that are bused across all the slots of an AXIe backplane.
- **AXIe Local Bus -** A set of 18, 42, or 62 signal pairs that connect adjacent slots.
- **CLK100 -** A set of 100 MHz LVDS signal pairs that is sourced by the *system module*, buffered on the AXIe backplane, and transmitted to all *instrument modules* in a star topology.
- **SYNC -** A set of LVDS trigger/synchronization signal pairs that is sourced by the *system module*, buffered on the AXIe backplane, and transmitted to all *instrument modules* in a star topology.
- **STRIG (Star Trigger) -** A set of bi-directional LVDS signal pairs that directly connects the *system slot* to all of the *instrument slots* in a star topology.
- **FCLK (Fabric Clock) -** A set of 100 MHz HCSL signal pairs that is sourced by the *system module*, buffered on the AXIe backplane, and transmitted to all *instrument modules* in a star topology. This fabric clock is the PCI Express® reference clock for all PCI Express® ports on the fabric channels connected to the system slot.

1.7.2 AdvancedTCA® Terms Applicable to AXIe

AXIe also incorporates many AdvancedTCA® terms. These terms are used as defined in the AdvancedTCA® specification. These include:
- **A1, A2**
- **Backplane**
- **Base Channel**
- **Base Interface**
- **Bottom**
- **Channel**
- **Component Side 1**
- **Component Side 2**
- **Dedicated Shelf Management Controller**
- **Dual Star Topology**
- **Electronic Keying (E-Keying)**
- **Fabric Channel**
- **Fabric Interface**
- **Face Plate**
- **Fan Tray**
- **Field Replaceable Unit (FRU)**
- **Field Replaceable Unit (FRU) Information**
- **GUID**
- **Handle (Face Plate Handle)**
- **Handle Switch**
- **Hardware Address**
- **IPM Controller (IPMC)**
- **IPMB**
- **IPMI**
- **K1, K2**
- **LAN**
- **Left**

- *Link*
- *Logic Ground*
- *Logical Slot*
- *LVDS*
- *MLVDS*
- *Payload*
- *Payload Interface*
- *Physical Address*
- *Physical Slot Number*
- *Port*
- *Rear Board or Rear Transition Module (RTM)*
- *Right*
- *RTM Subrack*
- *Shelf FRU Information*
- *Shelf Manager*
- *Shelf Manager IP Address*
- *ShMC*
- *ShMC Cross Connect*
- *Slot*
- *Star*
- *Subrack*
- *Top*
- *Zone 1*
- *Zone 1 Connector*
- *Zone 2*
- *Zone 2 Connector*
- *Zone 3*
- *Zone 3 Connector*

1.7.3 AdvancedTCA® Terms Not Applicable to AXIe

Some AdvancedTCA® terms are not used to describe similar AXIe entities/capabilities because they are different from the comparable terms most familiar within the test and measurement industry. These terms include:

- *Frame* - AdvancedTCA® term for an equipment *Rack.*
- *Front Board* - Equivalent to an AXIe *Module.*
- *Hub Board* - Equivalent to an AXIe *System Module.*
- *Hub Slot* - Equivalent to an AXIe *System Slot.*
- *Node Board* - Equivalent to an AXIe *Instrument Module.*
- *Node Slot* - Equivalent to an AXIe *Instrument Slot.*
- *Shelf* - Equivalent to an AXIe *Chassis.*

2. AXIe Mechanical Requirements

AXIe modules and chassis are required to conform to the relevant mechanical requirements of AdvancedTCA®. A few of the AdvancedTCA® requirements are not relevant to AXIe and are specifically excluded. These include references to the RTMs, Zone 3 interconnects, and sound power levels.

2.1 General Mechanical Requirements

AXIe products are required to conform to all of the requirements included in Section 2.1 of the AdvancedTCA® specification.

RULE 2.1: AXIe-1 products SHALL conform to AdvancedTCA® Requirements 2.1-2.7.

2.2 AXIe Module Mechanical Requirements

AXIe modules conform to the mechanical requirements for AdvancedTCA® front boards. AXIe-1 systems do not include rear transition modules (RTMs), so AXIe-1 modules have no need for Zone 3 connectors. However, the AXIe-3.n extension specifications are permitted to implement Zone 3 interconnects. To prevent interference with the Zone 3 interconnects and possible damage to modules, the K2 alignment/keying feature is retained for AXIe-1 modules. A default K2 key value is specified for AXIe-1 modules. For cases where AXIe-3.n Zone 3 extensions do not incorporate the K2/A2 alignment/keying feature and utilize VHDM connectors with integral alignment pins, an additional component keep out area in Zone 3 is specified for AXIe-1 modules. This keep out area is shown in Figure 2.1. AXIe-1 modules are not permitted to implement the optional zone 3 PCB extension defined in Figure 2-7 of the AdvancedTCA® specification, in order to prevent interference with AXIe-3.n Zone 3 connectors.

RULE 2.2: AXIe-1 modules SHALL conform to AdvancedTCA® Requirements 2.8, 2.10-2.75, 2.80-2.105, and 2.133, subject to the additional restrictions of this specification.

RULE 2.3: AXIe-1 module PCBs SHALL NOT implement the optional Zone 3 PCB extension defined in AdvancedTCA® Requirement 2.9.

PERMISSION 2.1: AXIe-1 module PCBs MAY implement the optional front-edge PCB extension defined in AdvancedTCA® Requirement 2.9.

RULE 2.4: AXIe-1 modules SHALL NOT have any components more than 5 mm tall mounted on the PC board's Component Side 1 within the additional component height restriction area shown in Figure 2-1.

OBSERVATION 2.1: The AXIe-3.1 Zone 3 backplane connectors each have an integral alignment pin. This pin extends into the AXIe-1 module envelope. RULE 2.4 provides clearance for this alignment pin.

OBSERVATION 2.2: AXIe-1 modules are not required to implement full hot swap capability. In particular, they are not required to implement the handle switch referenced by AdvancedTCA® Requirement 2.76, nor are they required to implement the Blue Hot-Swap LED.

PERMISSION 2.2: AXIe-1 modules MAY support full hot swap capability and implement the handle switch in accordance with AdvancedTCA® Requirement 2.76.

RULE 2.5: AXIe-1 modules that include a handle switch to support full hot swap capability SHALL conform to AdvancedTCA® Requirements 2.76-2.79.

RULE 2.6: An AXIe-1 module that does not have a handle switch SHALL provide a virtual handle switch input to the module's IPM controller indicating that the switch is always in the closed position.
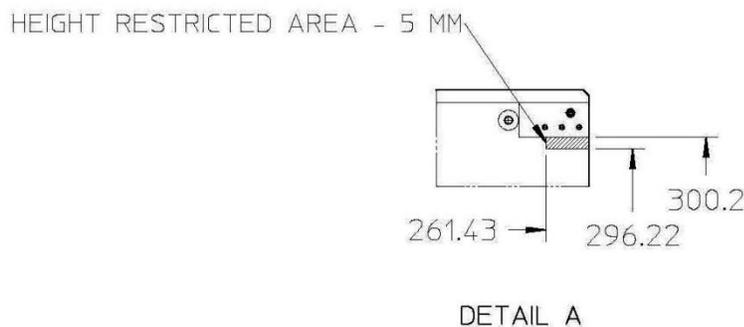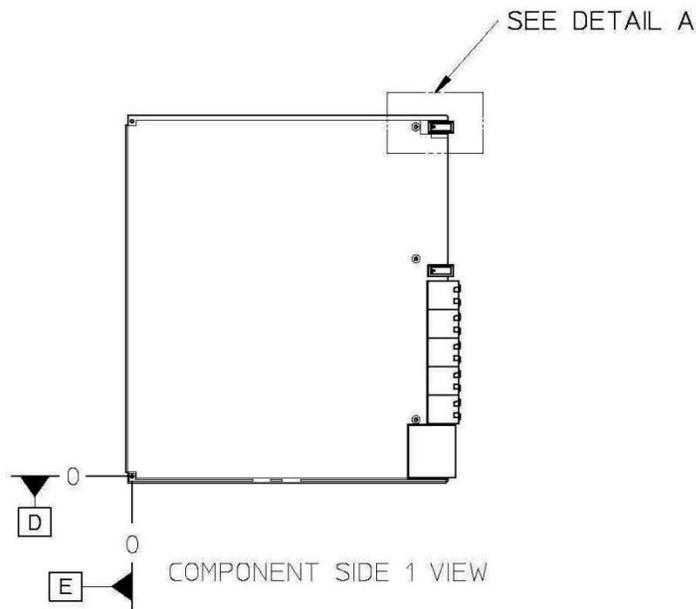
Figure 2-1: Additional component height restriction area for AXIe-1 modules.

2.2.1 AXIe Front Panel LEDs and Labels

AXIe-1 modules are not required to implement any of the AdvancedTCA® front panel LEDs, other than the AdvancedTCA®-defined LED 1. It is up to the module manufacturers to choose the locations of any front panel LEDs, and the colors of any LEDs other than the required LED 1. Because of the dense IO needs for test and measurement, it is suggested that the LEDs be located near the top and bottom of the module faceplate.

PERMISSION 2.3: AXIe-1 modules MAY conform to AdvancedTCA® Requirements 2.106-2.132.

RULE 2.7: An AXIe-1 module that implements full hot-swap capability SHALL have a BLUE front panel LED that that conforms to AdvancedTCA® Requirements 2.112 – 2.113.

RULE 2.8: Each AXIe-1 module SHALL have a front panel LED 1 that conforms to AdvancedTCA® Requirements 2.115 – 2.118.

2.3 Rear Transition Modules

The AXIe-1 Architecture does not include the use of Rear Transition Modules or module connections to Zone 3 connectors. Section 2.3 of the AdvancedTCA® specification, "RTM assembly" is not applicable to AXIe-1.

RULE 2.9: AXIe-1 modules SHALL NOT have any Zone 3 connectors.

2.4 AXIe Backplane Connectors

The AXIe architecture includes the AdvancedTCA® Zone 1 and Zone 2 connectors. Certain Telecom-specific signals on the Zone 1 connector are not used in AXIe. Signals specified for the AXIe Zone 2 connector include features that are not part of AdvancedTCA®.

2.4.1 Zone 1 Connector

AXIe-1 devices and systems utilize the power, platform management, and hardware addressing connections provided on the Zone 1 connector. AXIe-1 does not include the metallic test and ringing generator connections.

RULE 2.10: AXIe-1 modules and backplanes SHALL conform to AdvancedTCA® Requirements 2.267-2.274, 2.297, and 2.299.

OBSERVATION 2.3: AXIe-1 systems are not required to implement redundant power or platform management bus connections. Modules and systems are required to implement and connect the "_A" resources. Use of the "_B" resources is optional.

The Zone 1 connector is defined in Appendix B of the AdvancedTCA® specification, with the physical dimensions of the front board connector shown in Table B.5. For better interoperability, AXIe requires that the connector pins have tighter tolerances.

RULE (2.0) 2.1: The front board Zone 1 connector pins having nominal 1.6 mm diameters (reference øE in AdvancedTCA® Table B.5) SHALL have diameters in the range 1.562 – 1.613 mm.

RULE (2.0) 2.2: The front board Zone 1 connector pins having nominal 0.76 mm diameters (reference øF in AdvancedTCA® Table B.5) SHALL have diameters in the range 0.749 – 0.775 mm.

2.4.2   Zone 2 Connector

AXIe-1 systems use the same Zone 2 connectors as AdvancedTCA®.

RULE 2.11: AXIe-1 modules and backplanes SHALL conform to AdvancedTCA® Requirements 2.300-2.302.

2.4.3 Zone 3 Connector

AXIe-1 systems do not use Zone 3 resources. However, the AXIe-3.n extension specifications are allowed to incorporate Zone 3 features appropriate for their respective marketplaces. The dimensions of AXIe-3.n Zone 3 midplane connectors are restricted to prevent interference with AXIe-1 modules. In addition, AXIe-1 chassis are required to mechanically accept AdvancedTCA® and AXIe-3.n modules that have Zone 3 connectors.

OBSERVATION 2.4: Future AXIe-3.n specifications that define zone 3 connections are expected to conform to AdvancedTCA® Requirements 2.303-2.313.

OBSERVATION 2.5: For compatibility with AXIe-1 modules, AXIe-3.n Zone 3 midplane connectors must fit within the Zone 3 Connector envelope defined by Figure 2-2. This applies only to midplane connectors, not to AXIe-3.n RTM connectors. The RTM connector envelope is defined by AdvancedTCA®. AdvancedTCA® mechanical keying prevents AXIe-1 modules from full insertion into slots that have RTMs installed, so no additional connector envelope restrictions are necessary.
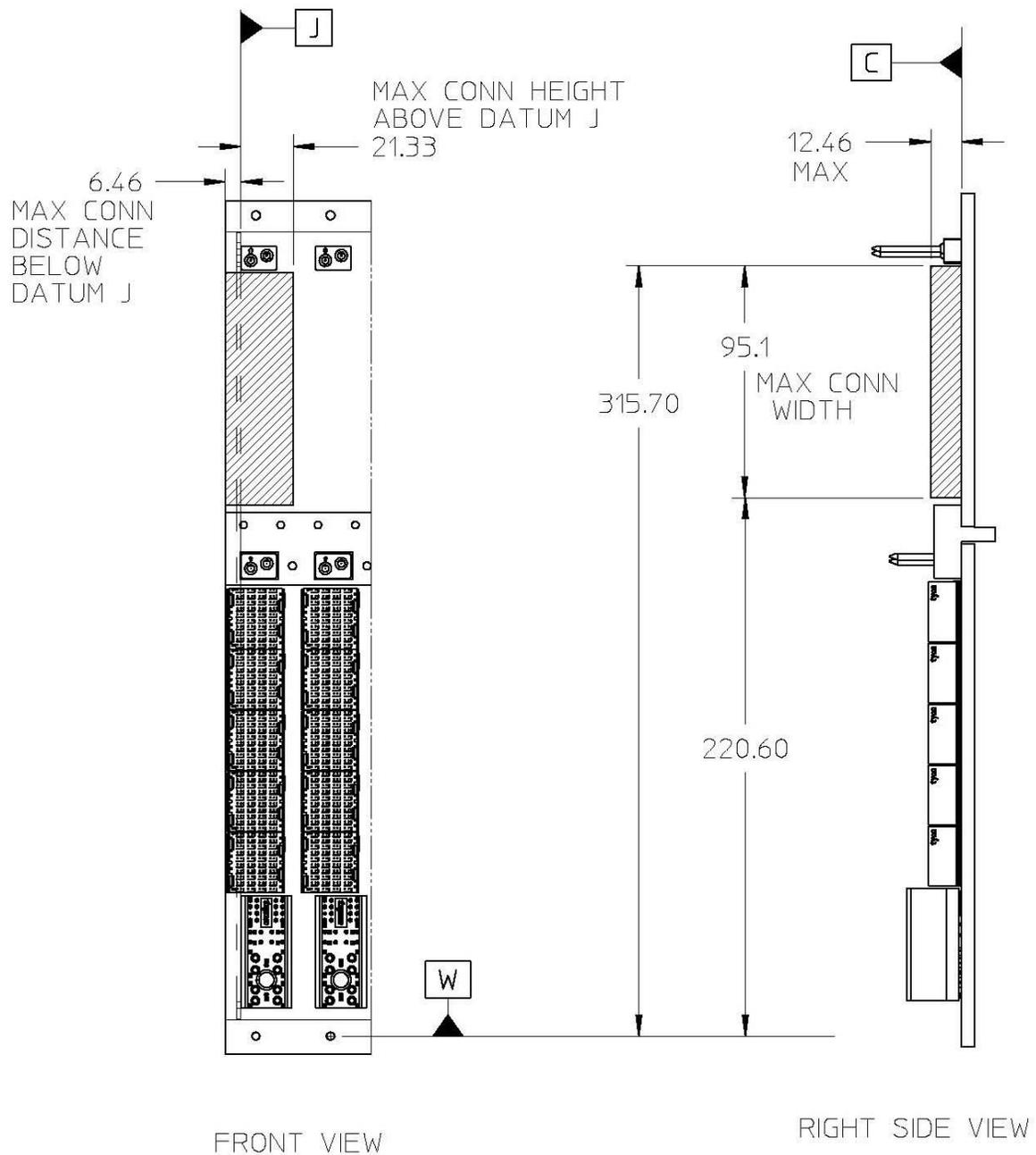
Figure 2-2: AXIe zone 3 midplane connector envelope.

2.4.4 Alignment and Keying

AXIe-1 Systems implement the AdvancedTCA® keying mechanism.

RULE 2.12: AXIe-1 modules and backplanes SHALL conform to AdvancedTCA® Requirements 2.314-2.324, 2.328-2.329, and 2.331-2.338.

AXIe-1 modules have no Zone 3 connectors and are designed to not interfere with any AXIe-3.n Zone 3 midplane connectors. The module must be keyed to prevent insertion into AdvancedTCA® slots that have incompatible Zone 3 RTM or midplane connectors. The default K2 key value for AXIe-1 modules is "5x", where the "x" represents a round hole in the receptacle that will accommodate any key value (1-8) (See Table AdvancedTCA® 2-14 for the definitions of the key values). AXIe-3.1 Zone 3 midplanes utilize connectors with integrated alignment pins. For these backplanes, the K2 alignment receptacle on AXIe-1 modules may need to be removed to prevent interference between the receptacle and the connector alignment pin. Future AXIe-3.n (where n>1) specifications that define zone 3 backplanes will provide A2 keying pins with value "5n".

RULE 2.13: AXIe-1 modules SHALL factory configure their K2 receptacles to the default key value "5x".

OBSERVATION 2.6: AdvancedTCA® Requirement 2.338 mandates that A2 and K2 keying be field reconfigurable.

2.5 Backplanes

AXIe-1 backplanes are permitted to mix open-system slot positions with proprietary features, such as slot positions for embedded system resources. The open-system slot positions of AXIe-1 backplanes are required to conform to AdvancedTCA® mechanical requirements. The AXIe architecture is optimized for subracks that can be mounted in standard 19" EIA racks. This limits the vertical slot count to 14, the maximum supported by the AXIe-1 architecture.

RULE 2.14: AXIe-1 open-system backplane slot positions SHALL conform to AdvancedTCA® Requirements 2.339 and 2.241-2.346.

RULE 2.15: AXIe-1 backplanes SHALL provide no more than 14 AXIe slots.

Having only 14 slots frees up fabric interface resources that in AdvancedTCA® are used for communication with slots 15-16. AXIe uses these pins on the hub 1 slot as Star Trigger connections. On the remaining slots, these pins are used for the AXIe local bus.

OBSERVATION 2.7: The numbering of any non-AXIe slots or other proprietary features is beyond the scope of this specification.

2.6 Subracks

AXIe-1 subracks support AXIe modules in conformance to AdvancedTCA® requirements for support of Front Boards. However AXIe-1 systems do not include Rear Transition Modules. As with backplanes, subracks are permitted to mix proprietary and open-system slots.

While AdvancedTCA® subracks are used in well established environmental conditions, it is anticipated that AXIe systems will be used in much broader environmental ranges. While designing subracks to the integrity tests in the AdvancedTCA® specification is prudent, it is up to the system integrator to determine the actual environmental conditions for AXIe systems. Consequently, the subrack integrity tests in the AdvancedTCA® specification are not required.

RULE 2.16: AXIe-1 open-system subrack slot positions SHALL conform to AdvancedTCA® Requirements 2.347, 2.349-2.351, 2.353-2.354, 2.357-2.364, 2.367, 2.369-2.386, 2.388, 2.390-2.397, 2.404-2.406, and 2.408.

2.7 AXIe Chassis

Beyond the subrack and backplane requirements, which assure compatibility with AXIe modules, there are no restrictions on the mechanical designs of AXIe chassis. Chassis features are manufacturer-specific. None of the requirements of the AdvancedTCA®'s section 2.7, "Shelf", apply to AXIe chassis.

OBSERVATION 2.8: This specification does not prohibit chassis features such AdvancedTCA® RTM subracks.

3. Hardware Platform Management

The AXIe architecture incorporates the hardware platform management features of AdvancedTCA®. AXIe systems are not required to support the complete hot swap capabilities of AdvancedTCA®. However, the module's FRUs are required to support all of the operational states required for AdvancedTCA® front boards. The only hardware difference is that AXIe modules are not required to have the handle switches that sense the module's insertion and impending removal from the chassis nor the blue hot-swap LEDs. Certain low power, simple modules are not required to support hardware platform management.

AXIe includes the use of PCI Express® on the fabric interface. AXIe modules that implement the PCI Express® fabric interface are subject to the additional requirements of the PICMG® 3.4 Revision 1.0 Specification, "PCI Express®/Advanced Switching for AdvancedTCA® Systems". The AXIe architecture also includes some platform management extensions that are important to the proper configuration of the PCI Express® fabric, the AXIe timing and trigger resources, and the AXIe local bus.

The AXIe trigger interface is not managed by electronic keying. It is the responsibility of host application software to manage the use of the AXIe trigger bus and ensure that no more than one device is driving the bus at a given time.

AXIe modules and chassis do not use the AdvancedTCA® bused resources (synchronization clock interface, metallic test bus, ringing bus). Thus AXIe equipment is not required to implement any of the associated AdvancedTCA® electronic keying requirements.

AXIe-1 chassis are required to include a dedicated shelf manager with a 10/100/1000BT LAN interface. This system manager interface may be routed either to the system slot's ShMC port or to an external connector. A redundant shelf manager is permissible, and the shelf manager(s) may have redundant LAN interfaces.

RULE 3.1: AXIe-1 modules and chassis SHALL conform to AdvancedTCA® Requirements 3.1-3.509 and 3.543-3.777, subject to the additional restrictions of this specification.

RULE 3.2: AXIe-1 modules that implement a PCI Express® fabric interface SHALL conform to the requirements of Chapter 4, "System Management" of PICMG® 3.4, subject to the additional restrictions of this specification.

RULE 3.3: Each AXIe-1 chassis SHALL include at least one dedicated shelf manager.

RULE 3.4: The required AXIe-1 chassis shelf manager SHALL provide at least one externally accessible IEEE 802.3 system manager interface, routed either to the system slot's ShMC port or to an external connector.

PERMISSION 3.1 An AXIe-1 chassis MAY implement dual-redundant shelf managers connected to a cross-connect ShMC port of the system slot, or to external LAN connectors, or both.

3.1 Electronic Keying

AXIe makes different use of some of the Zone 2 resources than AdvancedTCA®. These resources have some specific E-keying requirements.

3.1.1 Electronic Keying Process

The AXIe electronic keying process is an extension of the AdvancedTCA electronic keying process. Because of AXIe's additional interfaces, the shelf manager uses additional IPMI commands to enable/disable the AXIe backplane interface ports. There are also some AXIe defined data records added to the shelf and module FRU information. These records describe the point-to-point connectivity of the AXIe timing interface and local bus interface, along with additional information about the PCIe channels. AXIe shelf managers use the *AXIe Set Port State* and *AXIe Get Port State* commands in addition to the AdvancedTCA *Set Port State* and *Get Port State* commands.

RULE 3.5: AXIe-1 chassis shelf FRU information SHALL include AXIe Backplane Point-to-Point Connectivity records that describe the local bus and timing interface connectivity, along with any fabric channel connectivity that meets the requirements for 5 GT/s or 8 GT/s PCIe® signals. Each of these fabric channels SHALL have exactly one (1) AXIe channel descriptor, based on the maximum bandwidth of the channel.

OBSERVATION 3.1: AXIe-1 fabric channel connectivity is also described in the required AdvancedTCA® Backplane Point-to-Point connectivity records. Channels that meet the 5 GT/s or 8 GT/s requirements will have both AXIe and AdvancedTCA® Backplane Point-to-Point connectivity descriptors.

RULE 3.6: AXIe module information SHALL include AXIe Board Point-to-Point Connectivity records that describe the module's local bus ports, timing interface ports, and any reverse, 5 GT/s capable, or 8 GT/s capable PCIe® port.

RULE 3.7: AXIe-1 chassis shelf FRU information SHALL include AXIe Board Point-to-Point Connectivity records, associated with hardware address 10h, that describe the FCLK, CLK100, and SYNC connections to the backplane signal distribution buffers.

RULE 3.8: IPM controllers in AXIe-1 modules that have connections to any of the AXIe timing interface or local bus ports or that have PCIe reverse, 5GT/s, or 8GT/s fabric channel connections SHALL support Electronic Keying via the "AXIe Set Port State" and AXIe Get Port State" commands.

RULE 3.9: AXIe-1 shelf managers and module IPM controllers' use of and response to the "AXIe Set Port State" command SHALL conform to the AdvancedTCA requirements 3.468 – 3.473 for use of and response to the "Set Port State" command.

3.1.2 Point-to-Point Link Connectivity

The AXIe architecture utilizes the channel based connectivity model of AdvancedTCA®. It includes the base and fabric channel types defined by AdvancedTCA®. It also includes a *Local Bus* channel type. The port characteristics are summarized in Table 3-1.

Channel Type	Channel Size	Pairs/Port	Maximum Ports/Channel	Channels/Slot
Base	4 pairs	4 pairs	1 Port	1-14 Channels
Fabric	8 pairs	2 pairs	4 Port	1-13 Channels
Local Bus	18 pairs	18 pairs	1 Port	0-2 Channels
	42 pairs	42 pairs	1 Port	0-2 Channels
	62 pairs	62 pairs	1 Port	0-2 Channels
Timing	1 pair	1 pair	1 Port	4 Channels

Table 3-1: AXIe point-to-point channel attributes.

3.1.3 Backplane Point-to-Point Link Connectivity Record

For the base and fabric interfaces, AXIe E-keying uses the AdvancedTCA® Backplane Point-to-Point Connectivity Record. However, this record format does not define slot descriptor records for the AXIe local bus, nor does it include a means of identifying fabric channels that are suitable for Generation 2 PCIe® (5 GT/s) or Generation 3 (8 GT/s) operation. The AXIe Backplane Point-to-Point Connectivity Record is used to describe the AXIe local bus connectivity as well as high-performance fabric channels. AXIe shelf FRU information includes both AdvancedTCA® and AXIe backplane point-to-point connectivity records. The AXIe backplane connectivity record, described in Table 3-2, is very similar to the AdvancedTCA® backplane connectivity record and includes many of the same field definitions.

Offset	Length	Definition
0	1	Record type ID (per AdvancedTCA®)
1	1	End of List/Version (per AdvancedTCA®)
2	1	Record Length (per AdvancedTCA®)
3	1	Record Checksum (per AdvancedTCA®)
4	1	Header Checksum (per AdvancedTCA®)
5	3	Manufacturer ID (per AdvancedTCA®). Use the AXIe Consortium's IANA Private Enterprise Number, 35609 (008B19h).
8	1	AXIe Record ID. Use the value 00h.
9	1	Record Format Version. Use 00h.
10	m	AXIe Point-to-Point Slot Descriptor List (format per AdvancedTCA®)

Table 3-2: AXIe Backplane Point-to-Point Connectivity Record.

Table 3-3 describes the format of the AXIe Point-to-Point Slot Descriptor.

Offset	Length	Definition
0	1	AXIe Point-to-Point Channel Type: 00h : Reserved 01h: 5 GT/s capable single port fabric interface 02h: 5 GT/s capable double port fabric interface 03h: 5 GT/s capable full channel fabric interface 04h: Reserved 05h: 8 GT/s capable single port fabric interface 06h: 8 GT/s capable double port fabric interface 07h: 8 GT/s capable full channel fabric interface 08h – 0Fh: Reserved 10h: AXIe 18-pair Local Bus Interface 11h: AXIe 42-pair Local Bus Interface 12h: AXIe 62-pair Local Bus Interface 13h-17h: Reserved 18h: AXIe Timing Interface 19h – FFh: Reserved
1	1	Slot Address (per AdvancedTCA®)
2	1	Point-to-Point Channel Count (per AdvancedTCA®)
3	3*n	Point-to-Point Channel Descriptors (format per AdvancedTCA®)

Table 3-3: AXIe Point-to-Point Slot Descriptor.

The Backplane Point-to-Point Channel Descriptor entries for the fabric channels are identical to the AdvancedTCA® Backplane Point-to-Point Channel Descriptors. The entries for the AXIe-defined interfaces are shown in Table 3-4.

Bits	Description
23:18	Reserved. Always 0.

17:13	Local Channel.
	    AXIe Local Bus:
	        1 (00001b): Left channel
	        2 (00010b): Right channel
	    AXIe Timing Interface:
	        1 (00001b): FCLK
	        2 (00010b): CLK100
	        3 (00011b): SYNC
	        4 (00100b): STRIG (Instrument slots only)
	        5 (00100b): CLK100_FB (System slot only)
	        7 (00111b) – 19 (10011b): STRIG(2) – STRIG(14) (System slot only)

12:8	Remote Channel.
	    For FCLK, CLK100, and SYNC the remote channel is the same as the local channel. For logical slot 1 (Hardware Address 41h), the actual remote channel is the value in this field. Otherwise, the actual remote channel is given by the equation: $C_R = (S_L - 40h) * 3 + C$, where
	        C_R is the actual remote channel number,
	        S_L is the local Slot Number value (offset 1 of the AXIe point-to-point slot descriptor), and
	        C is the remote channel value specified in this field.

7:0	Remote Slot. Always 10h for FCLK, CLK100, and SYNC. This indicates connection to a backplane buffer instead of a remote slot.

Table 3-4: AXIe Point-to-Point Channel Descriptor.

RULE (2.0) 3.1: The AXIe Timing Interface FCLK, CLK100, and SYNC channels SHALL be described in the AXIe point-to-point slot descriptors associated with the physical AXIe slots.

OBSERVATION (2.0) 3.1: Within the backplane point-to-point connectivity record, there is no AXIe point-to-point slot descriptor associated with the backplane FCLK, CLK100, and SYNC buffers (at hardware address 10h). Thus the channels to the buffers must be described in each slot's AXIe point-to-point slot descriptor.

OBSERVATION (2.0) 3.2: The remote channel field is not wide enough to accommodate the range (0-42) of actual channel designations of the signals at the backplane buffers. Thus the actual remote channel is derived from the given value as specified in in Table 3-4.

3.1.4 AdvancedTCA® Board Point-to-Point Connectivity Record

For the base and many fabric interfaces on single-slot modules, AXIe E-keying uses the AdvancedTCA® Board Point-to-Point Connectivity Record, as defined by the AdvancedTCA® specification.

3.1.5 Extended AdvancedTCA® Board Point-to-Point Connectivity Record

The AdvancedTCA® E-keying scheme does not make provision for front boards that make connections to the Zone 2 connectors in multiple, adjacent slots. Such modules must use the Extended AdvancedTCA® Board Point-to-Point Connectivity record for those interfaces that are normally described by the standard AdvancedTCA® Board Point-to-Point Connectivity Record. The Extended AdvancedTCA® Board Point-to-Point Connectivity record, described in Table 3-5, includes a field that indicates the relative slot position of the Zone 2 connector interface described by the record. Single-slot AXIe modules may use either the standard AdvancedTCA® Board Point-to-Point Connectivity Record or the Extended AdvancedTCA® Board Point-to-Point Connectivity Record to describe the relevant interfaces. Note that unlike the standard AdvancedTCA® Board Point-to-Point Connectivity Record, the Extended AdvancedTCA Board Point-to-Point Connectivity record is defined as an AXIe OEM record and carries the AXIe Manufacturer ID in the header.

Offset	Length	Definition
0	1	Record type ID (per AdvancedTCA®)
1	1	End of List/Version (per AdvancedTCA®)
2	1	Record Length (per AdvancedTCA®)
3	1	Record Checksum (per AdvancedTCA®)
4	1	Header Checksum (per AdvancedTCA®)
5	3	Manufacturer ID (per AdvancedTCA®). Use the AXIe Consortium's IANA Private Enterprise Number, 35609 (008B19h).
8	1	AXIe Record ID. Use the value 02h.
9	1	Record Format Version. Use 00h.
10	1	Physical Slot Number (relative to the IPMC's physical slot number "n") 00h: Physical slot n 01h: Physical slot $n+1$ 02h: Physical slot $n+2$ … 0Eh: Physical slot $n+14$ 0Fh: Physical slot $n+15$ 10h –EFh: Reserved F0h: Physical slot $n-16$ F1h: Physical slot $n-15$ … FEh: Physical slot $n-2$ FFh: Physical slot $n-1$
11	1	OEM GUID Count (per AdvancedTCA®)
12	16*n	OEM GUID List (per AdvancedTCA®)
12+ 16*n	m	Link Descriptor List (format per AdvancedTCA®)

Table 3-5: Extended AdvancedTCA Board Point-to-Point Connectivity Record.

RULE (2.0) 3.2: A multiple-slot AXIe module SHALL use the Extended AdvancedTCA® Board Point-to-Point Connectivity Record for all of its relevant base and fabric interfaces.

PERMISSION (2.0) 3.1: A single-slot AXIe module MAY use either the standard or Extended AdvancedTCA® Board Point-to-Point Connectivity Record for its relevant base and fabric interfaces.

3.1.6 AXIe Board Point-to-Point Connectivity Record

For the base and fabric interfaces, AXIe E-keying uses the AdvancedTCA® Board Point-to-Point Connectivity Record. However, this record format does not define link descriptor records for the AXIe local bus, nor does it include a means of distinguishing between PCIe® upstream-facing and downstream-facing ports or between PCIe® 2.5, 5, and 8 GT/s ports. . The AXIe Board Point-to-Point Connectivity Record is used to describe the AXIe local bus, FCLK, CLK100, SYNC, and STRIG ports, as well as certain PCIe® fabric ports. AXIe module FRU information includes both AdvancedTCA® and AXIe board point-to-point connectivity records. AXIe shelf FRU information also includes board point-to-point connectivity records for its FCLK, CLK100, and SYNC signal distribution buffers. The AXIe board connectivity record has 2 versions, which are very similar to the AdvancedTCA® backplane connectivity record and includes many of the same field definitions. Version 00, for single-slot AXIe modules is described in Table 3-6. Version 01, for single-slot or multiple-slot AXIe modules is described in Table 3-7.

Offset	Length	Definition
0	1	Record type ID (per AdvancedTCA®)
1	1	End of List/Version (per AdvancedTCA®)
2	1	Record Length (per AdvancedTCA®)
3	1	Record Checksum (per AdvancedTCA®)
4	1	Header Checksum (per AdvancedTCA®)
5	3	Manufacturer ID (per AdvancedTCA®). Use the AXIe Consortium's IANA Private Enterprise Number, 35609 (008B19h).
8	1	AXIe Record ID. Use the value 01h.
9	1	Record Format Version. Use 00h.
10	1	OEM GUID Count (per AdvancedTCA®)
11	16*n	OEM GUID List (per AdvancedTCA®)
11+ 16*n	m	Link Descriptor List (format per AdvancedTCA®)

Table 3-6: Single-slot AXIe Board Point-to-Point Connectivity Record (version 00).

AXIe modules may span multiple backplane slots. In order for a multi-slot module's single IPMC controller to participate in E-keying for all of the module's boards, each board's point-to-point connectivity record must include relative slot information. The Version 01 AXIe board point-to-point connectivity record is used to describe each board's connectivity for all of its AXIe Local Bus, FCLK, CLK100, SYNC, and STRIG ports, as well as certain PCIe® fabric ports A multi-slot AXIe module's FRU information is required to include a Version 01 AXIe Board Point-to-Point Connectivity Record for each board within the module.

Offset	Length	Definition
0	1	Record type ID (per AdvancedTCA®)
1	1	End of List/Version (per AdvancedTCA®)
2	1	Record Length (per AdvancedTCA®)
3	1	Record Checksum (per AdvancedTCA®)
4	1	Header Checksum (per AdvancedTCA®)
5	3	Manufacturer ID (per AdvancedTCA®). Use the AXIe Consortium's IANA Private Enterprise Number, 35609 (008B19h).
8	1	AXIe Record ID. Use the value 01h.
9	1	Record Format Version. Use 01h.
10	1	Physical Slot Number (relative to the IPMC's physical slot number "*n*")

		00h: Physical slot *n*
		01h: Physical slot *n*+1
		02h: Physical slot *n*+2
		…
		0Eh: Physical slot *n*+14
		0Fh: Physical slot *n*+15
		10h –EFh: Reserved
		F0h: Physical slot *n*- 16
		F1h: Physical slot *n*- 15
		…
		FEh: Physical slot *n*- 2
		FFh: Physical slot *n*- 1
11	1	OEM GUID Count (per AdvancedTCA®)
12	16*n	OEM GUID List (per AdvancedTCA®)
12+ 16*n	m	Link Descriptor List (format per AdvancedTCA®)

Table 3-7: Multiple-slot AXIe Board Point-to-Point Connectivity Record (version 01).

The AXIe Board Point-to-Point connectivity record's Link Descriptor entries have the same format as the AdvancedTCA® Link Descriptors and is shown in Table 3-8. However the values of the Link Designator, Link Type, and Link Type Extension fields are different, as shown in Table 3-9, Table 3-10, Table 3-11, Table 3-12, Table 3-13, and Table 3-14.

Bit field	*Description*
31:24	Link Grouping ID (per AdvancedTCA®)
23:20	Link Type Extension (per AdvancedTCA®)
19:12	Link Type (per AdvancedTCA®)
11:0	Link Designator (per AdvancedTCA®)

Table 3-8: AXIe Link Descriptor.

Bit field	*Description*
11	Port 3 Bit Flag (per AdvancedTCA®)
10	Port 2 Bit Flag (per AdvancedTCA®)
9	Port 1 Bit Flag (per AdvancedTCA®)
8	Port 0 Bit Flag (per AdvancedTCA®)
7:6	Interface. 00b: Fabric Interface 01b: AXIe Local Bus Interface 10b: AXIe Timing Interface 11b: Reserved

5:0	Channel Number.
	    Fabric Interface: Values per AdvancedTCA®
	    AXIe Local Bus:
	        01h: Left Channel
	        02h: Right Channel
	    AXIe Timing Interface (AXIe Instrument Modules):
	        01h: FCLK
	        02h: CLK100
	        03h: SYNC
	        04h: STRIG
	    AXIe Timing Interface (AXIe System Modules):
	        01h: FCLK
	        02h: CLK100

	03h: SYNC
	05h: CLK100_FB
	07h – 13h: STRIG(2) – STRIG(14)
	AXIe Timing Interface (Backplane buffers):
	01h: FCLK input from Logical Slot 1
	02h: CLK100 input from Logical Slot 1
	03h: SYNC input from Logical Slot 1
	04h, 07h, 0Ah, 0dh, 10h, 13h,16h, 19h, 1Ch, 1Fh, 22h, 25h, 28h, 2Bh: FCLK outputs to Logical Slots 1-14
	05h, 08h, 0Bh, 0Eh, 11h, 14h, 17h, 1Ah, 1Dh, 20h, 23h, 26h, 29h, 2Ch: CLK100 outputs to Logical Slots 1-14
	06h, 09h, 0Ch, 0Fh, 12h, 15h, 18h, 1Bh, 1Eh, 21h, 24h, 27h, 2Ah, 2Dh: SYNC outputs to Logical Slots 1-14

Table 3-9: AXIe Link Designator.

Type	Description
00h	Reserved
01h	AXIe PCIe® Fabric Link
02h	AXIe FCLK
03h	AXIe CLK100
04h	AXIe SYNC
05h	AXIe STRIG
06h - EFh	Reserved
F0h - FEh	E-Keying OEM GUID Definition (per AdvancedTCA®)
FFh	Reserved

Table 3-10: AXIe Link Type.

Type	Definition
0h	Reserved
1h	2.5 GT/s reverse link
2h	5 GT/s normal link
3h	5 GT/s reverse link
4h	8 GT/s normal link
5h	8 GT/s reverse link
6h - Fh	Reserved

Table 3-11: AXIe Link Type Extension values when the AXIe Interface Type is 00b (Fabric Interface) and the AXIe Link Type is 01h (AXIe PCIe ®).

Type	Definition
0h	Reserved
1h	System slot output link.
2h	Instrument slot input.
3h - Fh	Reserved

Table 3-12: AXIe Link Type Extension values when the AXIe Interface Type is 10b (Timing Interface) and the AXIe Link Type is 02h (AXIe FCLK), 03h (AXIe FCLK), or 04h (AXIe FCLK).

Type	Definition
0h	Reserved
1h	All STRIG links

2h - Fh	Reserved

Table 3-13: AXIe Link Type Extension values when the AXIe Interface Type is 10b (Timing Interface) and the AXIe Link Type is 05h (AXIe STRIG).

Type	Definition
0h	Reserved
1h	18-pair AXIe Local Bus
2h	42-pair AXIe Local Bus
3h	62-pair AXIe Local Bus
4h - Fh	Reserved

Table 3-14: AXIe Link Type Extension values when the AXIe Interface Type is 01b (AXIe Local Bus Interface).

OBSERVATION 3.2: There are no AXIe defined local bus link types. Local bus link types are always OEM-defined.

RULE (2.0) 3.3: A multiple-slot AXIe module SHALL use Version 01 of the AXIe Board Point-to-Point Connectivity Record for all of its relevant AXIe interfaces.

PERMISSION (2.0) 3.2: A single-slot AXIe module MAY use either Version 00 or Version 01 of the AXIe Board Point-to-Point Connectivity Record for its relevant AXIe interfaces.

3.1.7 PCI Express® Electronic Keying

The AdvancedTCA® specifications make no provision for the fact that the PCI Express® interface is not inherently a peer-to-peer fabric. Each port can be characterized as either upstream-facing or downstream-facing. Connections are only valid between upstream-downstream port pairs. The situation is further complicated by the fact that a PCIe® domain may have only one root port. In other words, a switch may have only one upstream-facing port (but multiple downstream-facing ports). AXIe-1 implements an electronic keying scheme that allows a system module's fabric switch to have any, or none, of its backplane fabric ports be the switch's upstream-facing port to a root complex that resides behind the PCIe® port of the corresponding instrument module. The AXIe electronic keying scheme also includes provisions for 2nd and 3rd generation PCIe® links that are capable of operation at 5 GT/s and 8 GT/s. 2.5 GT/s PCIe ports that have the most common configuration (upstream-facing on instrument modules, or downstream facing on the system module) will use the E-keying defined by PICMG® 3.4. PCIe® ports that have reverse capabilities (downstream facing on instrument modules, or upstream-facing on the system module) and/or support faster data transfer rates will identify those capabilities using the AXIe-defined electronic keying extensions.

RULE 3.10: PCIe® upstream-facing ports on any fabric channel of a system module and PCIe® downstream-facing ports on channels 1 or 2 of instrument modules SHALL be designated as Reverse Links in AXIe electronic keying link descriptors.

OBSERVATION 3.3: All other PCIe® ports are defined as Normal Links. 2.5 GTs Normal Links use the link types defined in PICMG 3.4.

OBSERVATION 3.4: Ports that have both normal and reverse capability will have link descriptors for both capabilities. Ports that support multiple data rates will have link descriptors for each supported combination of normal/reverse capability and data rate.

OBSERVATION 3.5: Normal 2.5 GT/s PCIe® ports are described by AdvancedTCA® link descriptors. Reverse, 5 GT/s, and 8 GT/s PCIe® ports are described by AXIe link descriptors.

RULE 3.11: AdvancedTCA® Requirements 3.487 – 3.490 SHALL apply across all of a board's AXIe and AdvancedTCA® point-to-point connectivity records.

AXIe-1 shelf managers need to consider both the AdvancedTCA® and AXIe connectivity records when validating PCIe® links. PCIe® ports and fabric channels that support 2nd and 3rd generation data rates will also support 1st generation speeds. Thus a shelf manager may see valid matches for a particular port in both the AdvancedTCA® and AXIe connectivity records, and may enable only one of those links.

OBSERVATION 3.6: The ordering of link descriptors inside the concatenation of all board point-to-point connectivity records (both AXIe and PICMG) in a module's FRU information defines the preference of link descriptors for E-keying. The order is from most preferred to least preferred. If an AXIe module's normal PCI Express port can be negotiated to both 5 GT/s and 2.5 GT/s, there would be two link descriptors for it, and the preferred option (most likely 5 GT/s) should be located before the less preferred one. Unfortunately, the 2.5 GT/s descriptor would be in a PICMG connectivity record, while the 5 GT/s descriptor would be in an AXIe connectivity record. In this case, the AXIe connectivity record containing the 5 GT/s link descriptor for this port must be ahead of the PICMG connectivity record containing the port's 2.5 GT/s link descriptor within the module's FRU information.

OBSERVATION 3.7: AdvancedTCA® Requirements 3.487 – 3.490 include an implicit requirement that the shelf manager may not validate more than one protocol over any backplane connection. In other words only one of a port's link protocols may be enabled at any time. This requirement holds whether the capabilities are listed in the board's AXIe point-to-point connectivity records, in the board's AdvancedTCA® point-to-point connectivity records, or in both. When validating PCIe® connections over fabric channels, the shelf manager has to consider the backplane fabric channel's capability as well as the port capabilities. As shown in Table 3-15, 5 GT/s ports can match only 5 GT/s or 8 GT/s backplane channels. Similarly, 8 GT/s ports can match only 8 GT/s channels.

Module PCIe Port Protocol			Compatible Backplane Channel Types	
Speed	**Link Type[1]**	**Link Type Extensions[2]**	**Speed**	**Channel Types[3]**
2.5 GT/s	PICMG 05h	Any	≥ 2.5 Gb/s	PICMG 08h, 09h, 0Ah AXIe 01h, 02h, 03h, 05h, 06h, 07h
2.5 GT/s	AXIe 01h	1h	≥ 2.5 Gb/s	PICMG 08h, 09h, 0Ah AXIe 01h, 02h, 03h, 05h, 06h, 07h
5 GT/s	AXIe 01h	2h, 3h	≥ 5 Gb/s	AXIe 01h, 02h, 03h, 05h, 06h, 07h
8 GT/s	AXIe 01h	4h, 5h	≥ 8 Gb/s	AXIe 05h, 06h, 07h

[1]PICMG Link Types are defined in AdvancedTCA® Table 3-52. AXIe Link Types are defined in Table 3-10.
[2]AXIe Link Type Extensions are defined in Table 3-11.
[3]PICMG Channel Types are defined in AdvancedTCA® Table 3-46. AXIe Channel Types are defined in Table 3-3.

Table 3-15: PCIe port and backplane channel compatibility.

RULE 3.12: When determining PCIe® port electronic key matches, a shelf manager SHALL match the backplane channel speed capability to the port speed capabilities in addition to the matching of each port's Link Designator, Link Type, and Link Type Extension required by AdvancedTCA® (as described in AdvancedTCA® section 3.7.2.3, paragraph 317).

OBSERVATION 3.8: Since each PCIe port's normal/reverse capability and data rate combination is listed as a separate link type, the shelf manager's link matching algorithm will validate only connections between ports that support compatible combinations. For example a Normal 5GT/s link will match only another Normal 5GT/s link. In this example of a Normal link match, the matched ports would be a downstream-facing system module port and an upstream-facing instrument module port.

OBSERVATION (3.0) 3-1: AXIe-1 permits 8-lane and 16-lane PCIe® links, which span multiple fabric channels. Electronic keying of such links will require the usage of Link Grouping IDs in the link descriptors.

The PICMG 3.4 specification requires that E-keys for PCIe links include all of the link widths supported. AXIe-1 retains this requirement for fabric channel 1. However, in order to reduce the number of E-keying records for a module that connects to multiple fabric channels, AXIe-1 has different requirements for fabric channels 2-4.

RULE (3.0) 3-1: For any fabric channel 2, 3, or 4 connection that supports a PCIe® x1, x2, or x4 link, an instrument module's board E-keying records SHALL indicate x4 support.

PERMISSION (3.0) 3-1: For any fabric channel 2, 3, or 4 connection that supports a PCIe® x1, x2, or x4 link, an instrument module's board E-keying records MAY omit indications of x1 and/or x2 support.

RULE (3.0) 3-2: In an integrated chassis, for any connection to an instrument slot's fabric channel 2, 3, or 4 that supports a PCIe® x1, x2, or x4 link, the embedded system module's board E-keying records SHALL indicate x4 support.

PERMISSION (3.0) 3-2: In an integrated chassis, for any connection to an instrument slot's fabric channel 2, 3, or 4 that supports a PCIe® x1, x2, or x4 link, the embedded system module's board E-keying records MAY omit indications of x1 or x2 support.

OBSERVATION (3.0) 3-2: The preceding pairs of rules and permissions rely on PCIe® link training to resolve the actual link width within a single fabric channel connection.

3.1.8 AXIe Timing Interface Electronic Keying

AXIe timing interface electronic keying provides for the matching of AXIe module timing interfaces with compatible AXIe backplanes. The electronic keying for the FCLK, CLK100, and SYNC channels differs from AdvancedTCA® in that it must take into account the active backplane signal distribution buffers. These buffers appear to the shelf manager to be in a slot that has the hardware address 10h (which is the active shelf manager's own address). The shelf manager validates timing interface connections in the normal AdvancedTCA® manner, matching each port's Link Designator, Link Type, and Link Type extension.

RULE 3.13: When determining AXIe timing interface port electronic key matches, a shelf manager SHALL match each port's Link Designator, Link Type, and Link Type Extension as required by AdvancedTCA® for point-to-point connections.

3.1.9 AXIe Local Bus Electronic Keying

AXIe local bus electronic keying provides for matching of OEM protocols at each end of the link, as well as matching of the backplane link width with the device port width. All Local bus Link Types are manufacturer-defined and identified with OEM GUIDs. The required link width is encoded in the Link Type Extension field. To determine an electronic keying match, the shelf manager must check that the Link Designator, OEM GUID Link Type, and Link Type Extension fields of both ports match, and that the backplane channel width is at least as wide as the 2 ports.

RULE 3.14: When determining AXIe local bus port electronic key matches, a shelf manager SHALL ensure that the backplane local bus channel has at least as many signal pairs as the modules' connected local bus channel ports, in addition to the matching of each port's Link Designator, Link Type, and Link Type Extension required by AdvancedTCA®.

3.1.10 Extended AdvancedTCA® Set Port State Command

For the base and many fabric interfaces on single-slot modules, AXIe E-keying uses the standard AdvancedTCA® Set Port State command, as defined the the AdvancedTCA® specification. In a multi-slot AXIe module, the IPMC must be capable of controlling the port states of all of the module's boards. This requires a more capable version of the Set Port State command. The Extended AdvancedTCA® Set Port State command includes the necessary relative slot addressing capability. This Extended AdvancedTCA® Set Port Port State command is defined in Table 3-16, and is used to enable/disable AdvancedTCA® base and fabric interface ports.

	Byte	*Data Field*
Request Data	1:3	AXIe Identifier. Indicates AXIe defined OEM/group extension command. Use the AXIe Consortium's IANA Private Enterprise Number, 35609 (008B19h).
	4:7	Link Info (per AdvancedTCA®)
	8	State (per AdvancedTCA®)
	9	Physical Slot Number (relative to the IPMC's physical slot number "*n*") 00h: Physical slot *n* 01h: Physical slot *n*+1 02h: Physical slot *n*+2 … 0Eh: Physical slot *n*+14

		0Fh: Physical slot *n*+15 10h –EFh: Reserved F0h: Physical slot *n*- 16 F1h: Physical slot *n*- 15 … FEh: Physical slot *n*- 2 FFh: Physical slot *n*- 1
Response Data	1	Completion Code (per AdvancedTCA®)
	2:4	AXIe Identifier. Indicates AXIe defined OEM/group extension command. Use the AXIe Consortium's IANA Private Enterprise Number, 35609 (008B19h).

Table 3-16: Extended AdvancedTCA® Set Port State Command.

The Extended AdvancedTCA Set Port State command is an AXIe-defined IPMI command that uses NetFn 2Eh with the AXIe Consortium's IANA Private Enterprise Number, 35609 (008B19h) and the command code 03h. The response uses NetFn 2Fh with the AXIe Consortium's IANA Private Enterprise Number, 35609 (008B19h) and the command code 03h.

RULE (2.0) 3.4: An AXIe module that provides any Extended AdvancedTCA® Board Point-to-Point Connectivity Records SHALL implement the Extended AdvancedTCA® Set Port Port State command for the ports described in its Extended AdvancedTCA® Board Point-to-Point Connectivity Records.

RULE (2.0) 3.5: An AXIe module SHALL implement both the standard AdvancedTCA® Set Port Port State command and the Extended AdvancedTCA® Set Port Port State command for its ports described in an Extended AdvancedTCA® Board Point-to-Point Connectivity Record with the Physical Slot Number of 00b.

RULE (2.0) 3.6: When sending a Set Port State command for a port described in a standard AdvancedTCA® Board Point-to-Point Connectivity Record, a shelf manager SHALL use the standard AdvancedTCA® Set Port State command,

PERMISSION (2.0) 3.3: When sending a Set Port State command for a port described in an Extended AdvancedTCA® Board Point-to-Point Connectivity Record with the Physical Slot Number of 00b, a shelf manager MAY use either the standard AdvancedTCA® Set Port State command or the Extended AdvancedTCA® Set Port State command,

3.1.11 Set AXIe Port State Command

Since AXIe supports the additional port types that are described in the AXIe Board Point-to-Point Connectivity records, a different version of the Set Port State command must be used. This Set AXIe Port State command is defined in Table 3-17, and is used to enable/disable AXIe Local Bus, AXIe Timing Interface, Reverse PCIe®, 5GT/s PCIe®, and 8 GT/s PCIe® port types. Note that the physical slot number (byte 9) is optional for single-slot modules.

	Byte	*Data Field*
Request Data	1:3	AXIe Identifier. Indicates AXIe defined OEM/group extension command. Use the AXIe Consortium's IANA Private Enterprise Number, 35609 (008B19h).
	4:7	AXIe Link descriptor (per Table 3-6)
	8	State (per AdvancedTCA®)
	(9)	Physical Slot Number (relative to the IPMC's physical slot number "*n*") Optional: Default = 00h 00h: Physical slot *n* 01h: Physical slot *n*+1 02h: Physical slot *n*+2 … 0Eh: Physical slot *n*+14 0Fh: Physical slot *n*+15 10h –EFh: Reserved F0h: Physical slot *n*- 16

		F1h: Physical slot *n*- 15 ... FEh: Physical slot *n*- 2 FFh: Physical slot *n*- 1
Response Data	1	Completion Code (per AdvancedTCA®)
	2:4	AXIe Identifier. Indicates AXIe defined OEM/group extension command. Use the AXIe Consortium's IANA Private Enterprise Number, 35609 (008B19h).

Table 3-17: Set AXIe Port State Command.

The Set AXIe Port State command is an AXIe-defined IPMI command that uses NetFn 2Eh with the AXIe Consortium's IANA Private Enterprise Number, 35609 (008B19h) and the command code 01h. The response uses NetFn 2Fh with the AXIe Consortium's IANA Private Enterprise Number, 35609 (008B19h) and the command code 01h.

RULE (2.0) 3.7: An AXIe module that provides any Version 01 AXIe Board Point-to-Point Connectivity Records SHALL implement Set AXIe Port State commands that include the Physical Slot Number field for the ports described in its Version 01 AXIe Board Point-to-Point Connectivity Records.

RULE (2.0) 3.8: When sending a Set AXIe Port State command for a port described in a Version 00 AXIe Board Point-to-Point Connectivity Record, a shelf manager SHALL send the command without including the Physical Slot Number field.

PERMISSION (2.0) 3.4: When sending a Set AXIe Port State command for a port described in a Version 01 AXIe Board Point-to-Point Connectivity Record, with the Physical Slot Number of 00b, a shelf manager MAY either include or omit the optional Physical Slot Number field.

3.1.12 Extended AdvancedTCA® Get Port State Command

For the base and many fabric interfaces on single-slot modules, AXIe E-keying uses the standard AdvancedTCA® Get Port State command, as defined the the AdvancedTCA® specification. In a multi-slot AXIe board, the IPMC must be capable of reporting the port states of all of the module's boards. This requires a more capable version of the Get Port State command. The Extended AdvancedTCA® Get Port State command includes the necessary relative slot addressing capability. This Extended AdvancedTCA® Get Port Port State command is defined in Table 3-18, and is used to report the state of AdvancedTCA® base and fabric interface ports.

	Byte	*Data Field*
Request Data	1:3	AXIe Identifier. Indicates AXIe defined OEM/group extension command. Use the AXIe Consortium's IANA Private Enterprise Number, 35609 (008B19h).
	4	Channel (per AdvancedTCA®)
	5	Physical Slot Number (relative to the IPMC's physical slot number "*n*") Optional: Default = 00h 00h: Physical slot *n* 01h: Physical slot *n*+1 02h: Physical slot *n*+2 ... 0Eh: Physical slot *n*+14 0Fh: Physical slot *n*+15 10h –EFh: Reserved F0h: Physical slot *n*- 16 F1h: Physical slot *n*- 15 ... FEh: Physical slot *n*- 2 FFh: Physical slot *n*- 1
Response Data	1	Completion Code (per AdvancedTCA®)

2:4	AXIe Identifier. Indicates AXIe defined OEM/group extension command. Use the AXIe Consortium's IANA Private Enterprise Number, 35609 (008B19h).
5:8	Link Info 1 (per AdvancedTCA®)
9	State 1 (per AdvancedTCA®)
10:13	Link Info 2 (per AdvancedTCA®)
14	State 2 (per AdvancedTCA®)
15:18	Link Info 3 (per AdvancedTCA®)
19	State 3 (per AdvancedTCA®)
20:23	Link Info 4 (per AdvancedTCA®)
24	State 4 (per AdvancedTCA®)

Table 3-18: Extended AdvancedTCA® Get Port State command.

The Extended AdvancedTCA® Get Port State command is an AXIe-defined IPMI command that uses NetFn 2Eh with the AXIe Consortium's IANA Private Enterprise Number, 35609 (008B19h) and the command code 04h. The response uses NetFn 2Fh with the AXIe Consortium's IANA Private Enterprise Number and the command code 04h.

RULE (2.0) 3.9: An AXIe module that provides any Extended AdvancedTCA® Board Point-to-Point Connectivity Records SHALL implement the Extended AdvancedTCA® Get Port Port State command for the ports described in its Extended AdvancedTCA® Board Point-to-Point Connectivity Records.

RULE (2.0) 3.10: An AXIe module SHALL implement both the standard AdvancedTCA® Get Port State command and the Extended AdvancedTCA® Get Port Port State command for its ports described in an Extended AdvancedTCA® Board Point-to-Point Connectivity Record with the Physical Slot Number of 00b.

RULE (2.0) 3.11: When sending a Get Port State command for a port described in a standard AdvancedTCA® Board Point-to-Point Connectivity Record, a shelf manager SHALL use the standard AdvancedTCA® Get Port State command,

PERMISSION (2.0) 3.5: When sending a Get Port State command for a port described in an Extended AdvancedTCA® Board Point-to-Point Connectivity Record with the Physical Slot Number of 00b, a shelf manager MAY use either the standard AdvancedTCA® Get Port State command or the Extended AdvancedTCA® Get Port State command,

3.1.13 Get AXIe Port State Command

There is also a Get AXIe Port State command for the AXIe defined ports, as shown in Table 3-19.

	Byte	*Data Field*
Request Data	1:3	AXIe Identifier. Indicates AXIe defined OEM/group extension command. Use the AXIe Consortium's IANA Private Enterprise Number, 35609 (008B19h).
	4	Channel (per AdvancedTCA®)
	(5)	Physical Slot Number (relative to the IPMC's physical slot number "*n*") Optional: Default = 00h 00h: Physical slot *n* 01h: Physical slot *n*+1 02h: Physical slot *n*+2 … 0Eh: Physical slot *n*+14 0Fh: Physical slot *n*+15 10h –EFh: Reserved F0h: Physical slot *n*- 16 F1h: Physical slot *n*- 15 … FEh: Physical slot *n*- 2 FFh: Physical slot *n*- 1

Response Data	1	Completion Code (per AdvancedTCA®)
	2:4	AXIe Identifier. Indicates AXIe defined OEM/group extension command. Use the AXIe Consortium's IANA Private Enterprise Number, 35609 (008B19h).
	5:8	AXIe Link descriptor 1(per Table 3-6)
	9	State 1 (per AdvancedTCA®)
	10:13	AXIe Link descriptor 1(per Table 3-6)
	14	State 2 (per AdvancedTCA®)
	15:18	AXIe Link descriptor 1(per Table 3-6)
	19	State 3 (per AdvancedTCA®)
	20:23	AXIe Link descriptor 1(per Table 3-6)
	24	State 4 (per AdvancedTCA®)

Table 3-19: Get AXIe Port State command.

The Get AXIe Port State command is an AXIe-defined IPMI command that uses NetFn 2Eh with the AXIe Consortium's IANA Private Enterprise Number, 35609 (008B19h) and the command code 02h. The response uses NetFn 2Fh with the AXIe Consortium's IANA Private Enterprise Number and the command code 02h.

RULE (2.0) 3.12: An AXIe module that provides any Version 01 AXIe Board Point-to-Point Connectivity Records SHALL implement the Get AXIe Port State command that includes the Physical Slot Number field for the ports described in its Version 01 AXIe Board Point-to-Point Connectivity Records.

RULE (2.0) 3.13: When sending a Get AXIe Port State command for a port described in a Version 00 AXIe Board Point-to-Point Connectivity Record, a shelf manager SHALL send the command without including the Physical Slot Number field.

PERMISSION (2.0) 3.6: When sending a Get AXIe Port State command for a port described in a Version 01 AXIe Board Point-to-Point Connectivity Record, with the Physical Slot Number of 00b, a shelf manager MAY either include or omit the optional Physical Slot Number field.

3.2 Intelligent Platform Management Bus

AXIe uses an intelligent platform bus (IPMB) for platform management communication between the intelligent FRUs (shelf manager, module IPMC, etc.) in a chassis. This IPMB conforms to the AdvancedTCA® requirements for IPMB-0, except that IPMB redundancy is not required.

RULE 3.15: AXIe-1 IPMs SHALL implement connections to IPMB-A.

PERMISSION 3.2: AXIe-1 IPMs MAY implement connections to IPMB-B.

3.3 Power Sequencing

AXIe-1 systems differ from AdvancedTCA® in that the chassis are normally AC-powered, and will be frequently powered up and down. This presents additional challenges for AXIe modules that contain computers having modern operating systems and disc-drive storage. In addition, the power-up sequence must support proper enumeration of the PCI Express subsystem, especially when some of the PCI Express endpoints are implemented in FPGAs or other devices that may not be immediately ready for training and enumeration. Thus, AXIe-1 includes sequencing requirements beyond those described in AdvancedTCA® section 3.2.4, "Managed FRU Operational State management".

AXIe power sequencing also addresses the fact that the AXIe E-keying protocols are not sufficient to unambiguously define the PCIe hierarchy. They include no mechanism to assure that only one of the System Module's PCIe ports is E-keyed as a reverse link if multiple host-capable modules are installed in the chassis. This is a problem because PCIe switches generally may have only one port facing upstream. The AXIe-1 power-sequencing scheme provides a mechanism to determine the PCIe host module(s) based on information stored in the system module.

3.3.1 Power-up Overview

An AXIe-1 system typically powers up in the following sequence:

1. External AC Power is applied to the power supply unit (PSU), which then applies DC power to the backplane 48 V power feeds.

2. The shelf manager executes its boot-up sequence and begins managing the FRU activation process.

3. Prior to or during the activation process, the shelf manager sends the Get AXIe Version query to each AXIe module's IPMC.

4. The shelf manager executes E-keying protocols for all of the AXIe modules except the System Module.

5. After E-keying for the other modules completes, the shelf manager executes E-keying protocols for the system module.

    a. The shelf manager retrieves the Root Channel Preference record from the System Module's IPMC.

    b. The shelf manager E-keys the System Module' fabric channels in the order specified by the Root Channel Preference List.

    c. Based on its capabilities and the information in the Root Channel Preference List, the System module accepts a reverse PCIe link assignment for one of its fabric channels.

    d. The shelf manager recognizes that the AXIe module attached to the reverse PCIe fabric channel is the PCIe host module.

6. The shelf manager executes the power management protocols for all of the AXIe modules, allowing the modules to start up.

7. Each AXIe module powers up and enable its PCIe interfaces, delaying its M3 (activation in progress) to M4 (active) state transition until it is ready for PCIe enumeration.

8. After all of the AXIe modules are in the M4 (active) FRU state, the shelf sends the Set PCIe Host State (enable) command to the PCIe host module.

9. Upon receipt of the Set PCIe Host State (enable) command, the selected PCIe host computer module begins PCI Express enumeration.

3.3.2 Power-down Overview

An AXIe-1 system generally powers down in the following sequence:

1. An operator presses the chassis' power button, which sends a "power-down" signal to the shelf manager.

2. The shelf manager deactivates all of the AXIe modules.

3. AXIe modules respond by executing orderly shutdowns.

4. After each module successfully shuts down, it indicates to the shelf manager that it is in the deactivated state.

5. Once all modules have deactivated, the shelf manager signals the PSU to remove power.

3.3.3 Root Channel Preference Record

The AXIe System Module includes a Root Channel Preference Record in its FRU information. This record indicates the user's preferences for which of the system module's fabric channels should be configured as a reverse PCIe link. The preferences are stored as fabric channel numbers in priority order. The Root Channel Preference Record is described in Table 3-20.

Offset	Length	Definition
0	1	Record type ID (per AdvancedTCA®)
1	1	End of List/Version (per AdvancedTCA®)
2	1	Record Length (per AdvancedTCA®)
3	1	Record Checksum (per AdvancedTCA®)

4	1	Header Checksum (per AdvancedTCA®)
5	3	Manufacturer ID (per AdvancedTCA®). Use the AXIe Consortium's IANA Private Enterprise Number, 35609 (008B19h).
8	1	AXIe Record ID. Use the value 03h.
9	1	Record Format Version. Use 00h.
10	1	Channel Preference List Count. This is the number entries, *c*, in the root channel preference list.

11	*c*	Root Channel Preference List. Each entry is one byte, in priority order (highest priority first). The list includes exactly one entry for every fabric channel supported by the System module plus one entry for the System module itself.
		  00h: Indicates the System Module.
		  01h – 0Dh: Fabric channels 1-13.
		  0Eh – FFh: Reserved.

Table 3-20: Root Slot Preference Record.

RULE (2.0) 3.14: An AXIe System Module's FRU information SHALL include a Root Channel Preference Record that includes a user configurable Root Channel Preference List.

3.3.4 Get AXIe Version Command

The Get AXIe Version command, shown in Table 3-21, is required for all AXIe modules. It is used by the shelf manager to both inform a module of its own AXIe-1 specification compliance level and to determine the AXIe-1 compliance level of the responding module.

	Byte	*Data Field*
Request Data	1:3	AXIe Identifier. Indicates AXIe defined OEM/group extension command. Use the AXIe Consortium's IANA Private Enterprise Number, 35609 (008B19h).
	4	Requestor's Major AXIe Revision. Use 02h.
	5	Requestor's Minor AXIe Revision. Use 00h.
Response Data	1	Completion Code (per AdvancedTCA®)
	2:4	AXIe Identifier. Indicates AXIe defined OEM/group extension command. Use the AXIe Consortium's IANA Private Enterprise Number, 35609 (008B19h).
	6	Responder's Major AXIe Revision. Use 02h.
	7	Responder's Minor AXIe Revision. Use 00h.

Table 3-21: Get AXIe Version Command

The Get AXIe Port State command is an AXIe-defined IPMI command that uses NetFn 2Eh with the AXIe Consortium's IANA Private Enterprise Number, 35609 (008B19h) and the command code 05h. The response uses NetFn 2Fh with the AXIe Consortium's IANA Private Enterprise Number and the command code 05h.

RULE (2.0) 3.15: An AXIe module SHALL implement the Get AXIe Version command.

3.3.5 Set PCIe Host State Command

The Set PCIe Host State command, defined in Table 3-22, is required for all AXIe host computer modules and is optional for all other modules. It controls when a host computer may begin PCI Express enumeration after power-on.

	Byte	*Data Field*
Request Data	1:3	AXIe Identifier. Indicates AXIe defined OEM/group extension command. Use the AXIe Consortium's IANA Private Enterprise Number, 35609 (008B19h).
	4	PCIe Enumeration State 00h: Disable 01h: Enable 02h-FFh: Reserved

Response Data	1	Completion Code (per AdvancedTCA®)
	2:4	AXIe Identifier. Indicates AXIe defined OEM/group extension command. Use the AXIe Consortium's IANA Private Enterprise Number, 35609 (008B19h).

Table 3-22: Set PCIe Host State Command.

The Set PCIe Host State command is an AXIe-defined IPMI command that uses NetFn 2Eh with the AXIe Consortium's IANA Private Enterprise Number, 35609 (008B19h) and the command code 06h. The response uses NetFn 2Fh with the AXIe Consortium's IANA Private Enterprise Number and the command code 06h.

3.3.6 AXIe Module Requirements

An AXIe module with a PCI Express endpoint treats its IPMC's transition from the M3 (FRU activation in progress) to the M4 (FRU activated) state as the equivalent of the end of a PCI Express fundamental reset (per section 6.6.1 of the PCI Express Base Specification). The implication is that the endpoint is capable of beginning link training within 20 ms. This enables the shelf manager to know when all PCIe endpoints are ready for the host controller to begin normal PCIe operations.

An AXIe module that is capable of acting as a PCI Express host computer (including a root complex and PCIe enumeration and configuration software) must support the Set PCIe Host State command. For backwards compatibility, such a module defaults at power-on to having its PCIe enumeration state enabled. While its PCIe enumeration state is disabled, a host computer module is not allowed to begin PCIe enumeration. Non-host modules are not required to support the Set PCIe Host State command.

RULE (2.0) 3.16: The IPMC for an AXIe module that has an upstream-facing PCI Express port SHALL NOT execute the M3 to M4 transition until all of the following conditions are true:

- **Its PCI Express ports that have been enabled as upstream-facing by E-keying are powered and configured.**
- **Its PCI Express ports are ready to commence link training within 20 ms and ready to process DLLPs (Data Link Layer Packets) and TLPs (Transaction Layer Packets) immediately thereafter, as required after a fundamental reset by the PCI Express base specification.**

RULE (2.0) 3.17: The IPMC for an AXIe module that has PCI Express host computer capability SHALL implement the Set PCIe Host State command to control its PCIe enumeration state. Its PCIe enumeration state SHALL default to "disabled" upon entering the M2 (Activation Request) FRU state.

RULE (2.0) 3.18: While an AXIe module's PCIe Enumeration state is "disabled", it SHALL NOT issue any configuration requests to its backplane PCIe port. It SHALL treat the transition of the PCIe enumeration state to "enabled" as the end of a conventional reset as described in the PCI Express Specification for purposes of beginning PCIe enumeration and configuration.

OBSERVATION (2.0) 3.3: Older shelf managers that do not comply with this version of the AXIe-1 specification may not send the Set PCIe Host State command to the PCIe host module. In such a case, the host module will never commence PCIe enumeration unless it implements a timeout. It is possible for a host module to recognize the presence of one of these older shelf manager versions, since such a shelf manager will not send the Get AXIe Version command to the module.

RECOMMENDATION (2.0) 3.1: When an AXIe module having PCIe host capability is powered up without having first received a Get AXIe Version command, it should wait for a user-configured timeout and then transition its PCIe Enumeration state to "enabled".

This specification allows a wide variety of AXIe system module capabilities and implementations. Thus it does not require a system module to implement any particular algorithm for selecting which fabric channel to enable as a reverse link during E-keying. However, it is anticipated that most system modules will implement a single PCIe switch fabric which may have a single upstream-facing PCIe port enabled for normal operation. This upstream-facing port may be to a backplane fabric channel, an external cable, or to some internal device. A simple algorithm is suitable for such devices. Note that the shelf manager will E-key the system module's fabric channels in the order that

they are listed in the Root Channel Preference List. The shelf manager will assign port states based on E-keying matches. Thus the system module should ordinarily accept the first reverse link channel assignment offered by the shelf manager, since that will be the first port in the root channel preference list for which both of the attached devices are capable of supporting a reverse link. Once it accepts any reverse link assignment it should reject all subsequent reverse link requirements. A value of 00h in the root channel preference list indicates that the system module itself is the preferred root at that priority level. Thus the system module should not accept any PCIe reverse link assignments for channels that are behind 00h in the list.

RECOMMENDATION (2.0) 3.2: During power-up E-keying, a system module's IPMC should accept the first PCIe reverse link assignment from the shelf manager that is for a fabric channel that appears before the value 00h in the Root Channel Preference List. It should reject all other PCIe reverse link assignments by returning a completion code of FFh to the Set Port State command making the assignment.

The AdvancedTCA® M6 FRU state provides for a module's orderly shutdown, so no additional AXIe requirements are necessary for normal module shut-down. However, surprise power removals are likely to occur in many AXIe systems. Thus AXIe modules need to be tolerant of such scenarios.

RULE (2.0) 3.19: AXIe modules SHALL be designed to survive, without permanent damage, sudden chassis PSU shutdowns.

RECOMMENDATION (2.0) 3.3: AXIe modules SHOULD be tolerant of sudden chassis PSU shutdowns. Modules SHOULD normally recover from any resultant problems, such as disk corruption, without any operator intervention.

3.3.7 Shelf Manager and Chassis Requirements

At chassis power-up, an AXIe shelf manager performs an orderly module activation, E-keying, power-up, and system initiation sequence. This sequence is designed to delay any installed host computer modules from beginning PCI Express enumeration until after all AXIe modules have fully powered up and are ready to respond to PCIe configuration requests, signaled by their M3 to M4 FRU state transitions. Note that the receipt of FRU hot swap event messages allows the shelf manager to track the FRU states of all the AXIe modules in the chassis. When the shelf manager detects that all of the AXIe modules have reached the M4 (activated) state, it may enable PCIe Express enumeration. Note that an AXIe module will not transition to the M4 state until after it is ready to process PCIe configuration requests. The shelf manager enables PCIe enumeration by sending the Set PCIe Host State (enable) command to each AXIe module.

The power up sequence includes provisions for the startup of modules that are not compliant to this version of the specification and are thus unable to fully participate in the defined protocols.

Note that the shelf manager has no control over the startup of external host computers. So some other mechanism, which is beyond the scope of this mechanism, must be used to ensure overall system sequencing. The mechanism could be as simple as requiring an operator to manually sequence the chassis and computer start-up, or it could involve a system manager entity that monitors the AXIe chassis and controls the host computer start-up.

AXIe equipment may be used in systems that include multiple AXIe chassis and/or other cabled PCI Express devices. Thus, an AXIe-resident host controller may serve as the root complex for PCI Express endpoints outside of its AXIe chassis. In this case, there should be a mechanism to delay the host controller start-up until the external PCI Express devices are ready for enumeration.

RULE (2.0) 3.20: During system power-up, an AXIe shelf manager SHALL send the Get AXIe Version command to each AXIe module's IPMC after the module enters the M2 (Activation Request) FRU state and before beginning power negotiation or E-keying protocols with that module. This may be either before or after the module's transition to the M3 (Activation in Progress) state. Any module that returns a completion code of C1h (invalid command) SHALL be treated as a non-AXIe module for the remainder of the power-up sequence. All other modules SHALL be treated as AXIe modules for the remainder of the power-up sequence.

RULE (2.0) 3.21: During system power-up an AXIe shelf manager SHALL execute normal AdvancedTCA power negotiation and E-keying protocols with all non-AXIe modules in the chassis.

RULE (2.0) 3.22: During system power-up, after each AXIe module transitions to the M3 state, an AXIe shelf manager SHALL commence E-keying of the module without performing power allocation for that module.

RULE (2.0) 3.23: During system power-up an AXIe shelf manager SHALL delay E-keying the AXIe System Module until after E-keying has completed for all other shelf manager activated modules in the chassis.

RULE (2.0) 3.24: During system power-up, before E-keying the AXIe System module, an AXIe shelf manager SHALL retrieve the Root Channel Preference record from that System Module.

RULE (2.0) 3.25: During system power up, an AXIe shelf manager SHALL E-key the system module's fabric channels in the order specified in the system module's root channel preference list, ignoring any channel value of 00h in that list.

RULE (2.0) 3.26: During system power-up, after completing E-keying of the AXIe System module, an AXIe shelf manager SHALL execute the power negotiation protocols with all AXIe modules in the chassis.

RULE (2.0) 3.27: During system power-up, an AXIe shelf manager SHALL send the Set PCIe Host State (enable) command to the AXIe System Module's module and to every module that has a reverse PCIe link enabled by E-keying, after all of the AXIe modules have entered the M4 (activated) FRU state and all other system-dependent readiness conditions have been satisfied (see RECOMMENDATION (2.0) 3.4).

RULE (2.0) 3.28: An AXIe shelf manager SHALL provide both an operator indication and a mechanism for notifying a system manager that all of the PCIe modules in the chassis have entered the M4 (FRU Active) FRU state.

RECOMMENDATION (2.0) 3.4: An AXIe chassis, together with its shelf manager, SHOULD provide a mechanism for an external entity to delay the shelf manager from sending the Set PCIe Host State (enable) command to the AXIe modules in the chassis. This can be used to ensure that external, cable attached, PCIe devices are ready for enumeration before the host controller begins PCIe enumeration and configuration.

At system power-down, the shelf manager responds to the power-button notification by sending deactivation requests to all of the AXIe modules in the chassis. It then waits for all of the modules to indicate that they have successfully deactivated before it may command the PSU to power-down the 48 V power feeds. Note that the shelf manager is not required to power-down the 48 V rails. Instead it may leave the system in a low-power standby state until the next power-button notification. Support of either of these (or any other) power-down modes is optional and vendor-dependent.

RULE (2.0) 3.29: An AXIe shelf manager SHALL have a mechanism to detect activation of the chassis' power button anytime the 48V power feeds are powered.

RULE (2.0) 3.30: When an AXIe shelf manager detects a power-button activation while it is either in the process of activating the chassis or while the chassis is fully activated, the shelf manager SHALL begin to deactivate the chassis (by sending Set FRU Activation (Deactivate FRU) commands to all of the AXIe modules).

RULE (2.0) 3.31: When an AXIe shelf manager detects a power-button activation while it is either in the process of deactivating the chassis or while the chassis is fully deactivated, the shelf manager SHALL begin to activate the chassis (by sending Set FRU Activation (Activate FRU) commands to all of the AXIe modules).

RULE (2.0) 3.32: In the course of a normal chassis deactivation, an AXIe shelf manager SHALL NOT cause the PSU to power-down the 48V power feeds until all AXIe modules have transitioned to the M1 (FRU inactive) state.

RECOMMENDATION (2.0) 3.5: While a chassis is deactivated, but has its 48 V power feeds energized, the shelf manager SHOULD assume the lowest possible power state that allows it to monitor system temperatures, control the chassis fans, and detect power button activations.

An AC powered AXIe chassis must have a momentary pushbutton that an operator may press to power-up/activate and deactivate/power-down the chassis. The power-button configuration is vendor dependent. At a minimum, the chassis must provide a mechanism to notify the shelf manager of power-button activation (presses). It may also have a

mechanism for the power-button to directly cause the PSU to energize the 48 V power feeds. In addition, the chassis may have other switches or disconnects for removing power from the chassis.

RULE (2.0) 3.33: An AXIe chassis SHALL provide a momentary power-on/off switch, along with a mechanism to notify the shelf manager when the switch has been activated.

RECOMMENDATION (2.0) 3.6: An AXIe chassis SHOULD also provide a mechanism to support a remote power switch circuit.

RECOMMENDATION (2.0) 3.7: An AXIe chassis SHOULD provide a mechanism for an operator to force a chassis power-down regardless of the FRU states of the AXIe modules.

3.4 Unmanaged Modules

The AXIe-1 specification allows for the inclusion of low power, simple AXIe-0 unmanaged modules. Modules that meet certain AXIe-0 defined requirements are permitted to not participate in system management. Such modules are allowed to consume and dissipate power in excess of 15 Watts per slot. **RULE (3.0) 3-3: An AXIe-1 chassis SHALL, either by default or by providing a mechanism for a system integrator to configure its power and cooling settings, accommodate the presence of AXIe-0 unmanaged modules, as defined by the AXIe-0 specification, in any or all of its slots.**

OBSERVATION (3.0) 3-3: An AXIe-0 unmanaged module has no IPM controller and proceeds automatically to its fully powered (M4 equivalent) state upon application of backplane power.

OBSERVATION (3.0) 3-4: It is the responsibility of the system integrator to ensure that the AXIe-1 chassis is configured to provide adequate airflow and cooling to every slot that contains an unmanaged AXIe-0 module, based on each unmanaged module's published power specifications. It is anticipated that such modules could dissipate up to 50 Watts per slot.

4. Power Distribution

The AXIe-1 power distribution architecture incorporates most of the features of the AdvancedTCA® power distribution scheme. AXIe-1 utilizes the same -48V backplane power rails as AdvancedTCA®. However, AXIe-1 does not require the use of redundant power resources. AXIe-1 chassis could be powered from any external power source, typically AC power mains.

RULE 4.1: AXIe-1 chassis SHALL distribute at least one DC power feed, using the "Feed A" resources, to each module slot.

RECOMMENDATION 4.1: AXIe-1 chassis SHOULD also distribute DC power using the "Feed B" resources.

PERMISSION 4.1: AXIe-1 chassis MAY distribute either the same power feed on both the "Feed A" and "Feed B" resources or redundant DC power feeds from different Power supply resources to the "Feed A" and "Feed B" resources.

RULE 4.2: AXIe-1 modules SHALL be capable of operating from the power received on their -48V_A connections.

RECOMMENDATION 4.2: AXIe-1 modules SHOULD also be capable of operating from power received on their -48V_B connections

RULE 4.3: AXIe-1 modules and chassis SHALL conform to AdvancedTCA® requirements 4.3-4.15, 4.32-4.62, 4.68-4.69, and 4.79-4.104

RULE 4.4: AXIe-1 modules SHALL operate normally from a backplane voltage of -53V to -45V

RULE 4.5: AXIe-1 chassis -48V power supplies SHALL provide -53V to -45V to each AXIe-1 slot, with no more than 500 mV (peak-to-peak) of ripple noise under all rated DC load conditions.

In addition, AXIe-1 power supplies should comply with the conducted EMC recommendations in Section 7.1.1, "Chassis and Power Supply Conducted Emissions and Susceptibility".

5. Thermal Requirements

The AXIe-1 architecture incorporates most of the relevant thermal requirements in Section 5 of the AdvancedTCA® specification.

RULE 5.1: AXIe-1 modules and chassis SHALL conform to AdvancedTCA® requirements 5.1-5.19, 5.33-5.36, 5.37 (excluding the requirement for the sound power limits), 5.38-5.60, 5.69-5.75, and 5.77-5.82.

It is not required that the chassis have provisions for air filters. If a chassis does include provisions for air filters, then it is required to meet the requirements for air filters specified by AdvancedTCA®.

6. Data Transport

AXIe-1 incorporates many of AdvancedTCA®'s data transport features, including the base and fabric interfaces. AXIe-1 also includes some extensions to and modifications of some of the data transport resources to better meet the needs of the test and measurement marketplace.

6.1 Zone 2 Connectors

The Zone 2 connectors provide pins for up to 200 differential pairs per slot, although most slots do not have all of the connectors populated. Instrument slots have:

- 4 signal pairs connected to base interface resources
- 8-32 signal pairs connected to fabric interface resources
- 18-124 signal pairs connected to local bus resources
- 12 signal pairs connected to the AXIe-1 trigger bus
- 4 signal pairs connected to the AXIe-1 timing interface

The system slot (logical slot 1) has:

- Up to 56 signal pairs connected to base interface resources
- Up to 104 signal pairs connected to fabric interface resources
- 12 signal pairs connected to the AXIe-1 trigger bus
- Up to 16 signal pairs connected to the AXIe-1 timing interfaceBackplane Requirements

For most resources, the AXIe-1 backplane requirements are identical to the AdvancedTCA® requirements. The data transport interfaces are supported on the zone 2 connectors:

- The AXIe trigger bus is on connector P20.
- The AXIe timing interface is on connector P20.
- The AXIe local bus is on connectors P20 and P23, and optionally P21 and P24.
- The fabric interface is on connectors P20, P21, P22, P23, and P24, as it is in AdvancedTCA®.
- The base interface is on connectors P23 and P24, as it is in AdvancedTCA®.

6.1.1 Backplane Topologies

AXIe backplanes have different topologies for their different interfaces.

6.1.1.1 Base Interface Topology

The base interface is a single star topology that uses only the Hub slot 1 star of the dual star topology specified by AdvancedTCA®.

6.1.1.2 Fabric Interface Topology

AdvancedTCA® defines and allows various fabric interface topologies. AXIe-1 backplanes use only the Hub slot 1 star of the dual star fabric topology defined by AdvancedTCA®. This provides a single fabric channel connection to each instrument module, which is sufficient to support a 4-lane PCI Express® link. Integrated chassis are permitted to provide 1, 2, 3, or 4 fabric channel connections to instrument modules, thus supporting up to 16 PCI Express® lanes, distributed among 1 to 4 PCIe links.

6.1.1.3 AXIe Local Bus Topology

The AXIe local bus is routed between adjacent instrument slots, other than logical slot 1, as shown in Figure 6-1. There are at least18 local bus pairs connecting slots 2 and 3, another 18 connecting slots 3 and 4, etc. Most slots have 2 local bus ports, one port to each adjacent slot. Backplanes may implement 18, 42, or 62 local bus pairs for each port. The right-side Local bus port, LBR[0-61] on physical slot N connects to the left-side local bus port, LBL[0-61], on physical slot N+1 (or physical slot N+2, if physical slot N+1 is logical slot 1).
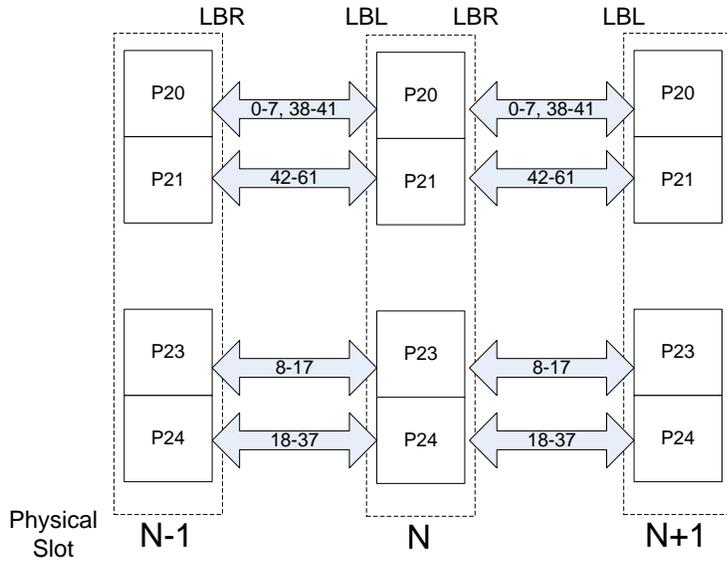
Figure 6-1: AXIe local bus backplane topology

6.1.1.4 AXIe Timing Interface Topology

The timing interface resources are all routed in star topologies from the system slot to the instrument slots. The routing and buffering requirements of the particular signals vary as appropriate to their use.

6.1.1.4.1 AXIe Fabric Clock

The AXIe Fabric Clock, FCLK, pair carries the reference clock signal for the PCI Express® signals on the Hub 1 fabric star. The FCLK signal is driven from the system slot and includes a backplane fan-out buffer to drive the FCLK signal pairs to each slot, as shown in Figure 1-5. There is no requirement for pair-to-pair length matching.

6.1.1.4.2 AXIe CLK100

The AXIe CLK100 pair carries a100 MHz measurement clock. The signal is driven from the system slot and includes a backplane fan-out buffer to drive the LVDS signal pairs to each slot, as shown in Figure 1-5. The CLK100 signals to each slot must have less than 100 ps skew from slot-to-slot.

6.1.1.4.3 AXIe SYNC

The AXIe SYNC pair carries a trigger/clock synchronization signal. The signal is driven from the system slot and includes a backplane fan-out buffer to drive the LVDS signal pairs to each slot, as shown in Figure Figure 1-5. The SYNC signals to each slot must have less than 100 ps skew from slot-to-slot.

6.1.1.4.4 AXIe STRIG

The AXIe STRIG pairs provide individual low-skew triggering between the system slot and each of the instrument slots. Each of these 13 pairs directly connects between slot 1 and another slot. The STRIG signals are not buffered on the backplane. The backplane STRIG signals to each slot must have less than 20 ps skew from slot-to-slot.

6.1.1.5 AXIe Trigger Bus Topology

The 12 AXIe trigger bus, TRIG[0-11] pairs are bused across all 14 slots, connecting to corresponding pins on each slot.

6.1.2 AXIe Zone 2 Routing Requirements

RULE 6.1: **AXIe 1.0AXIe-1 backplanes SHALL conform to AdvancedTCA® requirements 6.2-6.6, 6.11, and 6.18, subject to the additional restrictions of this specification.**

RULE 6.2: **AXIe-1 backplanes SHALL route the Hub 1 slot's base interface channels to all other slots.**

RULE 6.3: **AXIe-1 backplanes SHALL NOT implement the Hub 2 base interface star.**

OBSERVATION 6.1: **[deleted]**

RULE 6.4: **AXIe-1 backplanes SHALL route the fabric interface as a single star with the System Slot (Logical slot 1) as the hub.**

PERMISSION (3.0) 6-1: **AXIe-1 backplanes in integrated chassis MAY route 1, 2, or 3 additional fabric channels between the embedded system module and each instrument module, using the slots' fabric channels 2, 3, and/or 4.**

OBSERVATION (3.0) 6-1: **The additional backplane fabric channels used depend on the implememtation of the embedded system module in the chassis.**

RULE (3.0) 6-1: **An AXIe-1 backplane in an integrated chassis that routes more than 1 fabric channel between the embedded system module and an instrument slot SHALL route all of the port 0, port 1, port 2, and port3 signal pairs of each of the channels to the instrument module.**

RULE 6.5: **AXIe-1 backplanes SHALL route 18 local bus pairs between each pair of physically adjacent slots that don't include the system slot (logical slot 1).**

RULE 6.6: If an AXIe-1 backplane's system slot is not physical slot 1, the backplane SHALL route 18 local bus pairs between the two slots that are physically adjacent to, and on each side of, the system slot.

PERMISSION 6.1: **AXIe-1 backplanes MAY route a total of 18, 42, or 62 local bus pairs between any of the slot pairs that are required to have local bus connections.**

OBSERVATION 6.2: **[deleted]**

OBSERVATION 6.3: **Implementing a 42 pair local bus segment requires that each of the connected slots have the P24 backplane connector. Implementing a 62 pair local bus segment requires that each of the connected slots have both the P24 and P21 connectors loaded.**

RULE 6.7: **AXIe-1 backplanes SHALL route sequentially numbered local bus pairs, beginning with pair 0, between each of the slot pairs that are required to have local bus connections.**

RULE 6.8: AXIe-1 backplanes SHALL route a FCLK pair from logical slot 1 to the input of a backplane fabric clock buffer and route FCLK pairs from each of the fabric clock buffer's outputs to each of the other slots on the backplane.

RULE 6.9: **AXIe-1 backplanes SHALL route a CLK100 pair from logical slot 1 to the input of a backplane fabric clock buffer and route CLK100 pairs from each of the fabric clock buffer's outputs to each of the slots on the backplane.**

RULE 6.10: **AXIe-1 backplanes SHALL route a SYNC pair from logical slot 1 to the input of a backplane fabric clock buffer and route SYNC pairs from each of the fabric clock buffer's outputs to each of the other slots on the backplane.**

RULE 6.11: **AXIe-1 backplanes SHALL route a STRIG pair from logical slot 1 to each of the other slots on the backplane.**

6.1.3 AXIe Zone 2 Electrical Requirements

RULE 6.12: **Base interface, fabric interface, and AXIe local bus pairs SHALL conform to the AdvancedTCA® requirements 6.20-6.25.**

RULE 6.13: **Fabric interface pairs SHALL conform to the AdvancedTCA® requirement 6.26.**

RULE 6.14: Base interface pairs SHALL conform to the AdvancedTCA® requirement 6.27.

RULE 6.15: AXIe Local Bus pairs SHALL have a matched delay of less than 20 ps across all of the implemented pairs.

RULE 6.16: AXIe FCLK, CLK100, SYNC100, and STRIG pairs SHALL conform to AdvancedTCA® requirements 6.23-6.25.

RULE 6.17: AXIe CLK100 signal paths, including the clock fan-out buffer, SHALL have propagation delays matched within 100 ps between any 2 paths.

RULE 6.18: AXIe SYNC signal paths, including the clock fan-out buffer, SHALL have propagation delays matched within 100 ps between any 2 paths.

RULE 6.19: The CLK100 and SYNC signal paths, including the clock fan-out buffers, SHALL have propagation delays matched within 500 ps between any CLK100 path and any SYNC path.

RULE 6.20: AXIe STRIG signal paths SHALL have propagation delays matched within 20 ps between any 2 paths.

RULE 6.21: AXIe TRIG signal routing SHALL conform to the AdvancedTCA® Synchronization Clock requirements 6.28 - 6.31.

6.2 Module Requirements

The AXIe-1 architecture includes 2 classes of modules, **System Modules** and **Instrument Modules.** System Modules are similar to AdvancedTCA® Hub Boards and always occupy the System Slot (Logical slot 1, or Hub 1 slot) in an AXIe-1 chassis. Instrument Modules are similar to AdvancedTCA® node boards and are installed in logical slots 2-14.

6.2.1 System Modules

AXIe-1 system modules provide a set of core resources to the instruments in an AXIe chassis. The system module typically includes fabric switches for the base and PCI Express® fabric interfaces, system reference clocks, trigger logic, and other optional features such as external LAN or PCI Express interfaces to a host computer. System modules are typically designed to work with chassis having a specific number of slots.

6.2.2 Instrument Modules

AXIe-1 instrument modules utilize the base and/or fabric interfaces for control and data transfer transactions. They may also utilize the AXIe trigger bus, AXIe local bus, and the AXIe timing interfaces for interactions with other instruments or host computers. The functionality of instrument modules is neither defined, nor constrained, by this specification. Instrument modules may include measurement hardware, signal generation hardware, host computers, signal processing hardware, external communication interfaces, etc.

6.2.3 Zone 2 Support Requirements for Modules

RULE 6.22: AXIe-1 modules SHALL conform to AdvancedTCA® requirements 6.32, 6.35, 6.37-38, 6.41, 6.43, 6.47, and 6.52.

6.2.3.1 System Module Requirements

RULE 6.23: AXIe-1 system modules SHALL support the base interface or the fabric interface, or both.

RECOMMENDATION 6.1: AXIe-1 system modules SHOULD support both the base and fabric interfaces.

RULE 6.24: AXIe-1 system modules that support the base interface SHALL support sequentially numbered base channels, beginning with channel 2.

RECOMMENDATION : AXIe-1 system modules SHOULD support the zone 2 ShMC port.

RULE 6.25: AXIe-1 system modules SHALL implement internal switching sufficient to provide connection paths between all supported base channels, including the backplane ShMC port (if supported).

RULE 6.26: AXIe-1 system modules SHALL provide an external LAN port that has a connection path to all supported base channels, including the backplane ShMC port (if supported).

PERMISSION 6.2: AXIe-1 system modules MAY include other LAN devices that have connection paths to the base channels.

RULE 6.27: AXIe-1 system modules that support the fabric interface SHALL implement PCI Express® on the fabric interface in compliance with the requirements of PICMG 3.4.

RULE 6.28: AXIe-1 system modules SHALL support sequentially numbered fabric channels, beginning with channel 1.

RULE 6.29: AXIe-1 system modules SHALL implement internal PCI Express® switching sufficient to provide connection paths between all supported base channels.

OBSERVATION (3.0) 6-2: Standard AXIe-1 system modules support a single fabric channel per instrument slot.

PERMISSION (3.0) 6-2: Embedded system modules MAY support 1, 2, 3, or 4 fabric channels to each instrument slot.

RULE (3.0) 6-2: An embedded system module that connects 4 fabric channels to an instrument slot SHALL utilize the fabric routed to the instrument slot's channels 1, 2, 3, and 4.

RULE (3.0) 6-3: An embedded system module that connects 2 fabric channels to an instrument slot and implements two (2) x1, x2, or x4 PCIe links to the instrument, SHALL implement one of the links on the fabric routed to the instrument slot's channel 1 and the other on the fabric routed to the instrument slot's channel 2 or on the fabric routed to the instrument slot's channel 3.

RULE (3.0) 6-4: An embedded system module that connects 2 fabric channels to an instrument slot and implements one (1) x8 PCIe link to the instrument, SHALL implement the link on the fabric routed to the instrument slot's channels 1 and 2.

RULE (3.0) 6-5: An embedded system module that connects 3 fabric channels to an instrument slot and implements three (3) x1, x2, or x4 PCIe links to the instrument, SHALL implement one of the links on the fabric routed to the instrument slot's channel 1, another on the fabric routed to the instrument slot's channel 2, and the other on the fabric routed to the instrument slot's channel 3.

RULE (3.0) 6-6: An embedded system module in an integrated chassis that connects 3 fabric channels to an instrument slot and implements one (1) x8 and one (1) x1, x2, or x4 PCIe® link to the instrument, SHALL implement the x8 PCIe® links on fabric routed to the instrument slot's fabric channels 1 and 2, and the x1, x2, or x4 link on the fabric routed to the instrument slot's channel 3.

RULE (3.0) 6-7: An embedded system module in an integrated chassis that connects 4 fabric channels to an instrument and implements at least one x8 PCIe® link to the instrument, SHALL implement one of the x8 PCIe® links on fabric channels that route to the instrument slot's fabric channels 1 and 2.

RECOMMENDATION 6.2: AXIe-1 system modules SHOULD provide an external PCI Express® port that has a connection path to all supported fabric channels.

PERMISSION 6.3: AXIe-1 system modules MAY include other PCI Express® devices that have connection paths to the fabric channels.

RULE 6.30: AXIe-1 system modules that support the fabric interface SHALL drive the FCLK pair with the 100 MHz PCI Express® reference clock.

RULE 6.31: An AXIe-1 system module SHALL operate all of its fabric ports from the same 100MHz PCI Express® reference clock that is routed to the fabric clock port.

RULE 6.32: AXIe-1 system modules SHALL support CLK100 and SYNC.

RECOMMENDATION 6.3: AXIe-1 system modules SHOULD provide a capability to derive the CLK100 signal from an external clock input.

RECOMMENDATION 6.4: AXIe-1 system modules SHOULD provide a capability to derive an external clock output signal from CLK100.

RULE 6.33: Each AXIe-1 system module SHALL provide a mechanism for application software to generate trigger signals on any of the TRIG, STRIG, and SYNC pairs.

RULE 6.34: Each AXIe-1 system module SHALL provide a mechanism for application software to sense signal states on any of the TRIG and STRIG pairs.

RULE 6.35: Each AXIe-1 system module SHALL provide a circuit that can route the input signal of any of the TRIG and STRIG signals to its driver of the SYNC output pair.

RULE 6.36: Each AXIe-1 system module SHALL provide a circuit that can route the input signal of any of the STRIG signals to a driver of any other STRIG output pair.

RECOMMENDATION 6.5: Each AXIe-1 system module SHOULD provide a circuit that can route an external trigger input signal to an output driver of any of its TRIG, STRIG, or SYNC pairs.

RECOMMENDATION 6.6: Each AXIe-1 system module SHOULD provide a circuit that can route the input signal of any of the TRIG or STRIG signals to an external trigger driver.

PERMISSION 6.4: System module functionality MAY be integrated into an AXIe-1 chassis in a proprietary manner.

6.2.3.2   Instrument Module Requirements

RECOMMENDATION 6.7: AXIe-1 instrument modules SHOULD support the base interface or the fabric interface, or both.

RULE 6.37: AXIe-1 instrument modules that support the base interface SHALL support base channel 1.

PERMISSION 6.5: AXIe-1 instrument modules MAY connect to fabric channel 1, fabric channels 1 and 2, fabric channels 1, and 3, fabric channels 1-3, or fabric channels 1-4.

RULE 6.38: AXIe-1 instrument modules that connect to any of the fabric channels 1-4 SHALL implement PCI Express® on the channels in compliance with the requirements of PICMG 3.4.

RULE 6.39: An AXIe-1 instrument module SHALL operate its PCI Express® fabric channel 1, 2, 3, and 4 ports from the same 100MHz PCI Express® reference clock that it receives from its FCLK port.

OBSERVATION (3.0) 6-3: The PICMG 3.4 specification requires that a single fabric channel have no more than 1 PCIe link. Thus a module that has multiple x1 or x2 links must implement each link on a different channel.

RULE (3.0) 6-8: An AXIe-1 instrument module that connects to two (2) fabric channels slot and implements two (2) x1, x2, or x4 PCIe links, SHALL implement one of the links on fabric channel 1 and the other on either fabric channel 2 or fabric channel 3.

RULE (3.0) 6-9: An AXIe-1 instrument module that connects to two (2) fabric channels and implements one (1) x8 PCIe link, SHALL implement the link on fabric channels 1 and 2.

RULE (3.0) 6-10: An AXIe-1 instrument module that connects to three (3) fabric channels and implements three (3) x1, x2, or x4 PCIe links, SHALL implement one of the links on fabric channel 1, another on fabric channel 2, and the other on fabric channel 3.

RULE (3.0) 6-11: An AXIe-1 instrument module that connects to three (3) fabric channels and implements one (1) x8 and one (1) x1, x2, or x4 PCIe® link, SHALL implement the x8 PCIe® link on fabric channels 1 and 2, and the x1, x2, or x4 link on fabric channel 3.

RULE (3.0) 6-12: An AXIe-1 instrument module that connects to 4 fabric channels and implements at least one x8 PCIe® link, SHALL implement one of the x8 PCIe® links on fabric channels 1 and 2.

PERMISSION 6.6: [deleted]

PERMISSION 6.7: AXIe-1 instrument modules MAY connect to any of the CLK100, SYNC, or STRIG pairs.

PERMISSION 6.8: AXIe-1 instrument modules MAY connect to any of the 12 AXIe TRIG pairs.

RECOMMENDATION 6.8: An AXIe-1 instrument module that includes a function that senses any one of the TRIG, STRIG, or SYNC pairs SHOULD include a multiplexer that makes all of TRIG, STRIG, or SYNC inputs accessible to that function.

RECOMMENDATION 6.9: An AXIe-1 instrument module that includes a function that drives any one of the TRIG or STRIG pairs SHOULD include a multiplexer that enables that function to drive any of the TRIG or STRIG pairs.

RECOMMENDATION 6.10: Each AXIe-1 instrument module SHOULD include the capability for the application program to invert each of its TRIG, STRIG, and SYNC inputs.

PERMISSION 6.9: An AXIe-1 instrument module MAY connect to either or both of its local bus ports.

PERMISSION 6.10: [deleted]

RECOMMENDATION 6.11: [deleted]

6.3 Zone 2 Connector Usage

AXIe-1 backplanes and modules use the same zone 2 connectors as AdvancedTCA® backplanes and modules. The pin assignments for the AXIe base and fabric channels are identical to the pinouts for the same resources in AdvancedTCA®. The pinouts for the AXIe-specific resources are given in the following sections.

6.3.1 System Module/Slot Zone 2 Pin Assignments

The system slot/module pinouts differ from AdvancedTCA® hub slot/module pinouts only in connector set P20/J20, shown in Table 6-1, which includes the connections to the AXIe trigger and timing interfaces.

Row	Interface	System Slot (Logical Slot 1) J20/P20 Connector Pairs							
		ab		cd		ef		gh	
1	Trigger	TRIG[0]+	TRIG[0]-	TRIG[1]+	TRIG[1]-	TRIG[2]+	TRIG[2]-	TRIG[3]+	TRIG[3]-
2	Trigger	TRIG[4]+	TRIG[4]-	TRIG[5]+	TRIG[5]-	TRIG[6]+	TRIG[6]-	FCLK+	FCLK-
3	Trigger	TRIG[7]+	TRIG[7]-	TRIG[8]+	TRIG[8]-	TRIG[9]+	TRIG[9]-	TRIG[10]+	TRIG[10]-
4	Timing	TRIG[11]+	TRIG[11]-	STRIG[2]+	STRIG[2]-	SYNC+	SYNC-	CLK100+	CLK100-
5	Timing	STRIG[3]+	STRIG[3]-	STRIG[4]+	STRIG[4]-	STRIG[5]+	STRIG[5]-	STRIG[6]+	STRIG[6]-
6	Timing	Rsvd*	Rsvd*	CLK100FB+	CLK100FB-	STRIG[7]+	STRIG[7]-	STRIG[8]+	STRIG[8]-
7	Timing	STRIG[9]+	STRIG[9]-	STRIG[10]+	STRIG[10]-	STRIG[11]+	STRIG[11]-	STRIG[12]+	STRIG[12]-
8	Timing	Rsvd*	Rsvd*	Rsvd*	Rsvd*	STRIG[13]+	STRIG[13]-	STRIG[14]+	STRIG[14]-
9	Fabric Channel 13	Tx2[13]+	Tx2[13]-	Rx2[13]+	Rx2[13]-	Tx3[13]+	Tx3[13]-	Rx3[13]+	Rx3[13]-
10		Tx0[13]+	Tx0[13]-	Rx0[13]+	Rx0[13]-	Tx1[13]+	Tx1[13]-	Rx1[13]+	Rx1[13]-

*Rsvd pins are reserved and are unconnected on both backplanes and modules.

Table 6-1: J20/P20 Pin assignments for the system slot (logical slot 1).

The J21/P21, J22/P22, J23/P23, and J24/P24 connector pinouts for AXIe-1 system modules are the same as defined for AdvancedTCA® hub boards.

6.3.2 Instrument Module/Slot Zone 2 Pin Assignments

AXIe-1 instrument modules also have all of their trigger and timing interface connections in the P20/J20 connector set, shown in Table 6-2. In addition, they have local bus connections spread across multiple zone 2 connectors. The minimal 18-pair local bus channels reside in P20/J20 and P23/J23, as shown in Table 6-2 and Table 6-5. The optional expansion of the local bus channels to 42 or 62 pairs requires the use of additional connectors. A 42 pair local bus

channel requires the inclusion of P24/J24, shown in Table 6-6. A 62 pair channel requires the inclusion of P24/J24 and P21/J21, shown in Table 6-6 and Table 6-3.

Row	Interface	Instrument Slot (Logical Slot 2-14) J20/P20 Connector Pairs							
		ab		cd		ef		gh	
1	Trigger	TRIG[0]+	TRIG[0]-	TRIG[1]+	TRIG[1]-	TRIG[2]+	TRIG[2]-	TRIG[3]+	TRIG[3]-
2	Trigger	TRIG[4]+	TRIG[4]-	TRIG[5]+	TRIG[5]-	TRIG[6]+	TRIG[6]-	FCLK+	FCLK-
3	Trigger	TRIG[7]+	TRIG[7]-	TRIG[8]+	TRIG[8]-	TRIG[9]+	TRIG[9]-	TRIG[10]+	TRIG[10]-
4	Timing	TRIG[11]+	TRIG[11]-	STRIG+	STRIG-	SYNC100+	SYNC100-	CLK100+	CLK100-
5	Local Bus	LBL[0]+	LBL[0]-	LBL[1]+	LBL[1]-	LBR[0]+	LBR[0]-	LBR[1]+	LBR[1]-
6	Local Bus	LBL[2]+	LBL[2]-	LBL[3]+	LBL[3]-	LBR[2]+	LBR[2]-	LBR[3]+	LBR[3]-
7	Local Bus	LBL[4]+	LBL[4]-	LBL[5]+	LBL[5]-	LBR[4]+	LBR[4]-	LBR[5]+	LBR[5]-
8	Local Bus	LBL[6]+	LBL[6]-	LBL[7]+	LBL[7]-	LBR[6]+	LBR[6]-	LBR[7]+	LBR[7]-
9	Local Bus	LBL[38]+	LBL[38]-	LBL[39]+	LBL[39]-	LBR[38]+	LBR[38]-	LBR[39]+	LBR[39]-
10	Local Bus	LBL[40]+	LBL[40]-	LBL[41]+	LBL[41]-	LBR[40]+	LBR[40]-	LBR[41]+	LBR[41]-

Table 6-2: J20/P20 Pin assignments for instrument slots (logical slots 2-14).

OBSERVATION 6.4: Local bus pairs LBL[38-41] and LBR[38-41] are not used in 18-pair local bus channels, and the corresponding pins are not connected.

Instrument modules and slots that have 62-pair local bus channels use the J21/P21 connectors for local bus connections. Other ordinary instrument modules and slots are not required to have J21/P21connectors.

Row	Interface	Instrument Slot (Logical Slot 2-14) J21/P21 Connector Pairs							
		ab		cd		ef		gh	
1	Local Bus	LBL[42]+	LBL[42]-	LBL[43]+	LBL[43]-	LBR[42]+	LBR[42]-	LBR[43]+	LBR[43]-
2	Local Bus	LBL[44]+	LBL[44]-	LBL[45]+	LBL[45]-	LBR[44]+	LBR[44]-	LBR[45]+	LBR[45]-
3	Local Bus	LBL[46]+	LBL[46]-	LBL[47]+	LBL[47]-	LBR[46]+	LBR[46]-	LBR[47]+	LBR[47]-
4	Local Bus	LBL[48]+	LBL[48]-	LBL[49]+	LBL[49]-	LBR[48]+	LBR[48]-	LBR[49]+	LBR[49]-
5	Local Bus	LBL[50]+	LBL[50]-	LBL[51]+	LBL[51]-	LBR[50]+	LBR[50]-	LBR[51]+	LBR[51]-
6	Local Bus	LBL[52]+	LBL[52]-	LBL[53]+	LBL[53]-	LBR[52]+	LBR[52]-	LBR[53]+	LBR[53]-
7	Local Bus	LBL[54]+	LBL[54]-	LBL[55]+	LBL[55]-	LBR[54]+	LBR[54]-	LBR[55]+	LBR[55]-
8	Local Bus	LBL[56]+	LBL[56]-	LBL[57]+	LBL[57]-	LBR[56]+	LBR[56]-	LBR[57]+	LBR[57]-
9	Local Bus	LBL[58]+	LBL[58]-	LBL[59]+	LBL[59]-	LBR[58]+	LBR[58]-	LBR[59]+	LBR[59]-
10	Local Bus	LBL[60]+	LBL[60]-	LBL[61]+	LBL[61]-	LBR[60]+	LBR[60]-	LBR[61]+	LBR[61]-

Table 6-3: J21/P21 Pin assignments for instrument slots (logical slots 2-14).

OBSERVATION 6.5: [deleted]

Instrument modules and slots that support connections to fabric channels 3 and/or 4 use the J22/P22 connectors. Other instrument modules and slots are not required to have J22/P22 connectors.

OBSERVATION (3.0) 6-4: There is currently no provision for standard AXIe-1 system modules or slots to support more than one (1) fabric channel connection to each instrument slot. This feature is available only in integrated chassis with embedded system modules.

Row	Interface	Instrument Slot (Logical Slots 2-14) J22/P22 Connector Pairs							
		ab		cd		ef		gh	
1	Reserved	Tx2[2]+	Tx2[2]-	Rx2[2]+	Rx2[2]-	Tx3[2]+	Tx3[2]-	Rx3[2]+	Rx3[2]-
2		Tx0[2]+	Tx0[2]-	Rx0[2]+	Rx0[2]-	Tx1[2]+	Tx1[2]-	Rx1[2]+	Rx1[2]-
3	Reserved	Tx2[1]+	Tx2[1]-	Rx2[1]+	Rx2[1]-	Tx3[1]+	Tx3[1]-	Rx3[1]+	Rx3[1]-
4		Tx0[1]+	Tx0[1]-	Rx0[1]+	Rx0[1]-	Tx1[1]+	Tx1[1]-	Rx1[1]+	Rx1[1]-
5	Reserved	Tx2[2]+	Tx2[2]-	Rx2[2]+	Rx2[2]-	Tx3[2]+	Tx3[2]-	Rx3[2]+	Rx3[2]-

6		Tx0[2]+	Tx0[2]-	Rx0[2]+	Rx0[2]-	Tx1[2]+	Tx1[2]-	Rx1[2]+	Rx1[2]-
7	Fabric	Tx2[1]+	Tx2[1]-	Rx2[1]+	Rx2[1]-	Tx3[1]+	Tx3[1]-	Rx3[1]+	Rx3[1]-
8	Channel 4	Tx0[1]+	Tx0[1]-	Rx0[1]+	Rx0[1]-	Tx1[1]+	Tx1[1]-	Rx1[1]+	Rx1[1]-
9	Fabric	Tx2[1]+	Tx2[1]-	Rx2[1]+	Rx2[1]-	Tx3[1]+	Tx3[1]-	Rx3[1]+	Rx3[1]-
10	Channel 3	Tx0[1]+	Tx0[1]-	Rx0[1]+	Rx0[1]-	Tx1[1]+	Tx1[1]-	Rx1[1]+	Rx1[1]-

Table 6-4: J22/P22 Pin assignments for instrument slots (logical slots 2-14).

Row	Interface	Instrument Slot (Logical Slots 2-14) J23/P23 Connector Pairs							
		ab		cd		ef		gh	
1	Fabric	Tx2[2]+	Tx2[2]-	Rx2[2]+	Rx2[2]-	Tx3[2]+	Tx3[2]-	Rx3[2]+	Rx3[2]-
2	Channel 2	Tx0[2]+	Tx0[2]-	Rx0[2]+	Rx0[2]-	Tx1[2]+	Tx1[2]-	Rx1[2]+	Rx1[2]-
3	Fabric	Tx2[1]+	Tx2[1]-	Rx2[1]+	Rx2[1]-	Tx3[1]+	Tx3[1]-	Rx3[1]+	Rx3[1]-
4	Channel 1	Tx0[1]+	Tx0[1]-	Rx0[1]+	Rx0[1]-	Tx1[1]+	Tx1[1]-	Rx1[1]+	Rx1[1]-
5	Base Channel 1	BI_DA1+ (TX1+)	BI_DA1- (TX1-)	BI_DB1+ (RX1+)	BI_DB1- (RX1-)	BI_DC1+	BI_DC1-	BI_DD1+	BI_DD1-
6	Local Bus	LBL[8]+	LBL[8]-	LBL[9]+	LBL[9]-	LBR[8]+	LBR[8]-	LBR[9]+	LBR[9]-
7	Local Bus	LBL[10]+	LBL[10]-	LBL[11]+	LBL[11]-	LBR[10]+	LBR[10]-	LBR[11]+	LBR[11]-
8	Local Bus	LBL[12]+	LBL[12]-	LBL[13]+	LBL[13]-	LBR[12]+	LBR[12]-	LBR[13]+	LBR[13]-
9	Local Bus	LBL[14]+	LBL[14]-	LBL[15]+	LBL[15]-	LBR[14]+	LBR[14]-	LBR[15]+	LBR[15]-
10	Local Bus	LBL[16]+	LBL[16]-	LBL[17]+	LBL[17]-	LBR[16]+	LBR[16]-	LBR[17]+	LBR[17]-

Table 6-5: J23/P23 Pin assignments for instrument slots (logical slots 2-14).

Row	Interface	Instrument Slot (Logical Slot 2-14) J24/P24 Connector Pairs							
		ab		cd		ef		gh	
1	Local Bus	LBL[18]+	LBL[18]-	LBL[19]+	LBL[19]-	LBR[18]+	LBR[18]-	LBR[19]+	LBR[19]-
2	Local Bus	LBL[20]+	LBL[20]-	LBL[21]+	LBL[21]-	LBR[20]+	LBR[20]-	LBR[21]+	LBR[21]-
3	Local Bus	LBL[22]+	LBL[22]-	LBL[23]+	LBL[23]-	LBR[22]+	LBR[22]-	LBR[23]+	LBR[23]-
4	Local Bus	LBL[24]+	LBL[24]-	LBL[25]+	LBL[25]-	LBR[24]+	LBR[24]-	LBR[25]+	LBR[25]-
5	Local Bus	LBL[26]+	LBL[26]-	LBL[27]+	LBL[27]-	LBR[26]+	LBR[26]-	LBR[27]+	LBR[27]-
6	Local Bus	LBL[28]+	LBL[28]-	LBL[29]+	LBL[29]-	LBR[28]+	LBR[28]-	LBR[29]+	LBR[29]-
7	Local Bus	LBL[30]+	LBL[30]-	LBL[31]+	LBL[31]-	LBR[30]+	LBR[30]-	LBR[31]+	LBR[31]-
8	Local Bus	LBL[32]+	LBL[32]-	LBL[33]+	LBL[33]-	LBR[32]+	LBR[32]-	LBR[33]+	LBR[33]-
9	Local Bus	LBL[34]+	LBL[34]-	LBL[35]+	LBL[35]-	LBR[34]+	LBR[34]-	LBR[35]+	LBR[35]-
10	Local Bus	LBL[36]+	LBL[36]-	LBL[37]+	LBL[37]-	LBR[36]+	LBR[36]-	LBR[37]+	LBR[37]-

Table 6-6: J24/P24 Pin assignments for instrument slots (logical slots 2-14).

6.3.2.1 Fabric Channel Port Mapping

The mapping of PCI Express® lanes to fabric channel ports is given in Table 6-7: PCI Express® lane to fabric channel port mapping.

PCI Express® Links	Fabric Interface															
	Channel 1 Port				Channel 2 Port				Channel 3 Port				Channel 4 Port			
	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
Width	x1, x2, x4															
Lane	0	1	2	3												
Width	x1, x2, x4								x1, x2, x4							
Lane	0	1	2	3					0	1	2	3				
Width	x1, x2, x4				x1, x2, x4											

Lane	0	1	2	3	0	1	2	3								
Width	x1, x2, x4				x1, x2, x4				x1, x2, x4							
Lane	0	1	2	3	0	1	2	3	0	1	2	3				
Width	x1, x2, x4				x1, x2, x4				x1, x2, x4				x1, x2, x4			
Lane	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
Width	x1, x2, x4, x8															
Lane	0	1	2	3	4	5	6	7								
Width	x1, x2, x4, x8								x1, x2, x4							
Lane	0	1	2	3	4	5	6	7	0	1	2	3				
Width	x1, x2, x4, x8								x1, x2, x4				x1, x2, x4			
Lane	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
Width	x1, x2, x4, x8								x1, x2, x4, x8							
Lane	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
Width	x1, x2, x4, x8, x16															
Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Table 6-7: PCI Express® lane to fabric channel port mapping.

6.4 Base Interface

The AXIe-1 base interface meets all the requirements of AdvancedTCA®, except that the backplane does not have the redundant base interface channels routed between logical slot 2 and the higher numbered slots. Instrument modules do not implement a LAN connection to base channel 2. The AXIe-1 base interface channel assignments are shown in Figure 6-2.
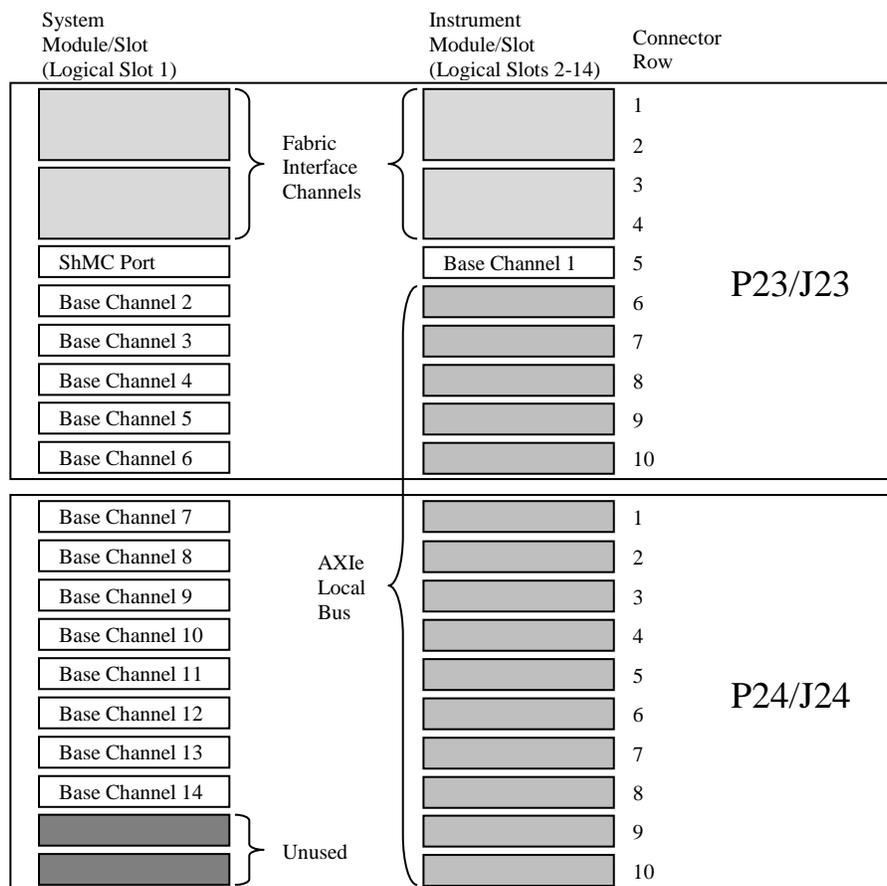
Figure 6-2: Base Interface Channel Assignments

RULE 6.40: AXIe-1 base channel implementations SHALL conform to AdvancedTCA® requirements 6.72-6.77.

Since AXIe-1 chassis include dedicated shelf managers, system slots and modules are required to include the ShMC port. This port meets all of the requirements of AdvancedTCA®.

RULE 6.41: AXIe-1 backplanes SHALL support the ShMC port at the system slot.

RULE 6.42: AXIe-1 backplane ShMC connections SHALL conform to the AdvancedTCA® requirements 6.62 – 6.65, 6.68, and 6.70 – 6.72.

RULE 6.43: AXIe-1 system modules SHALL support the ShMC connection either by mapping a single 10/100/1000BASE-T connection to the ShMC port, or as a ShMC cross connect by mapping two 10/100BASE-TX connections to the ShMC port.

The base interface channels have the same electrical design requirements as AdvancedTCA®.

RULE 6.44: AXIe-1 module base interface connections SHALL conform to the AdvancedTCA® requirements 6.74 – 6.77.

6.5 Fabric Interface Requirements

The fabric interface is always routed as a single star in AXIe-1 backplanes, as described in the AdvancedTCA® specification's Table 6-12, "Dual Star Backplane routing assignments", except that the backplane does not have the redundant fabric interface channels routed between logical slot 2 and the higher numbered slots. AXIe-1 modules use

PCI Express® connections on the system module's fabric star. All fabric channels and connections meet the electrical requirements of AdvancedTCA®, except that the ac-coupling capacitors are on the transmit (instead of receive) end of the channels (as required by the PCI Express® specifications). The PCI Express® connections also meet the requirements of PICMG® 3.4.

RULE 6.45: AXIe-1 module fabric interface connections SHALL conform to the AdvancedTCA® requirements 6.78, 6.79, and 6.80 – 6.89.

OBSERVATION 6.6: PICMG® 3.4 imposes additional signal integrity requirements on the PCI Express® connections.

RULE (2.0) 6.1: Fabric interface PCI Express® drivers SHALL be capacitively coupled to their backplane connector pins.

RULE (2.0) 6.2 Fabric interface PCI Express® receivers SHALL be directly connected to their backplane connector pins.

AXIe-1 modules and backplanes are permitted to support 5.0 GT/s signal rates as defined by the PCI Express® Base Specification. The 5.0 GT/s channels are subject to the signal integrity requirements of the PCI Express® specifications.

RULE 6.46: Any module fabric connection or backplane routing channel that claims 5.0 GT/s PCIe® compliance SHALL meet the signal integrity requirements for 5 GT/s operation as defined in the PCI Express® Base Specification and the PCI Express® Card Electromechanical Specification.

6.6 AXIe Timing Interface Requirements

The AXIe Timing Interface provides connections between each instrument module and central timing resources located in the system module. These signals include a bi-directional star trigger, STRIG; a point-to-point trigger/synchronization output from the system module, SYNC; an instrumentation reference clock, CLK100; and a fabric PCIe® reference clock, FCLK.

6.6.1 STRIG

The star trigger resource consists of up to 13 BLVDS pairs, STRIG(2:14). Each signal pair STRIG(n)+/STRIG(n)- connects the system slot to logical slot n. The backplane trace delays are matched within 20 ps across all STRIG pairs to provide a very low-skew trigger resource to multiple slots. The use of a STRIG pair by any particular instrument module is entirely application dependent. The backplane electrical design requirements for the star trigger pairs are given in Section 6.1.3, "AXIe Zone 2 Electrical Requirements". The star trigger topology and module connections are illustrated in Figure 6-3.
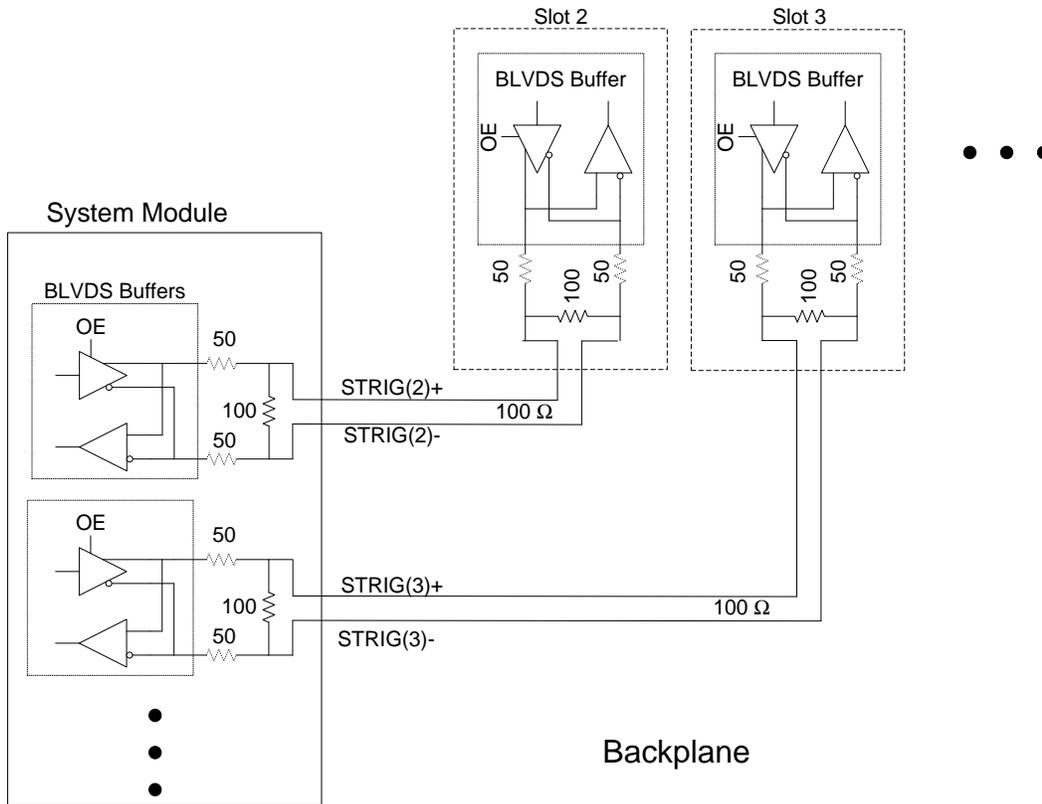
Figure 6-3: Typical STRIG Implementation

AXIe STRIG signals are managed by the electronic keying protocols and by application software. The shelf manager uses the electronic keying process to determine the compatibility of STRIG ports and enables a module to drive its STRIG port under application control. It is the responsibility of application software to determine which modules are permitted to drive any particular STRIG pair at a given time. Modules always power up with their STRIG drivers disabled. A module may not actively drive its STRIG port until both the shelf manager and the host application have enabled it

RULE 6.47: STRIG transmitters and receivers SHALL conform to the electrical requirements for BLVDS transmitters and receivers.

RULE 6.48: Modules that connect to a STRIG pair SHALL terminate that pair with a 100 Ω ±10% resistor across the signal pair as shown in Figure 6-3.

PERMISSION 6.11: Modules MAY include series terminations of ≤55 Ω on their STRIG connections as shown in Figure 6-3.

RULE 6.49: AXIe-1 modules SHALL be able to independently enable/disable their STRIG drivers.

RULE 6.50: AXIe-1 module STRIG drivers SHALL default to the disabled state at module power-on, and remain disabled until enabled by both the shelf manager and host application software.

RECOMMENDATION 6.12: AXIe-1 modules SHOULD treat the STRIG signals as active-high and/or positive-edge triggers, where the "high" is a valid logic state in which STRIG(n)+ is at a more positive voltage than STRIG(n)-.

RECOMMENDATION 6.13: AXIe-1 module functions that make use of received STRIG signals SHOULD have the programmable capability to effectively invert the sense of the received STRIG signal.

6.6.2 SYNC

The AXIe synchronization/trigger resource consists of up to 14 LVDS pairs, SYNC(1:14), along with a set of low-skew backplane signal distribution buffers. The signal pair SYNC(1)+/SYNC(1)- connects the system module's LVDS output to the backplane LVDS signal distribution buffers. Each signal pair SYNC(n)+/SYNC(n)- (where $1 < n \leq 14$) connects a buffer output pair to the LVDS input at logical slot n. The path delays (including SYNC(1), the backplane buffers, and SYNC(n) are matched within 100 ps across all SYNC paths to provide a low-skew trigger resource to multiple slots. The SYNC path delays are also matched within 500 ps of each CLK100 path. Thus the SYNC signals may operate synchronously with the CLK100 signals. The use of a SYNC pair by any particular instrument module is entirely application dependent. The backplane electrical design requirements for the synchronization/trigger pairs are given in Section 6.1.3, "AXIe Zone 2 Electrical Requirements". The SYNC topology and connections are illustrated in Figure 6-3.
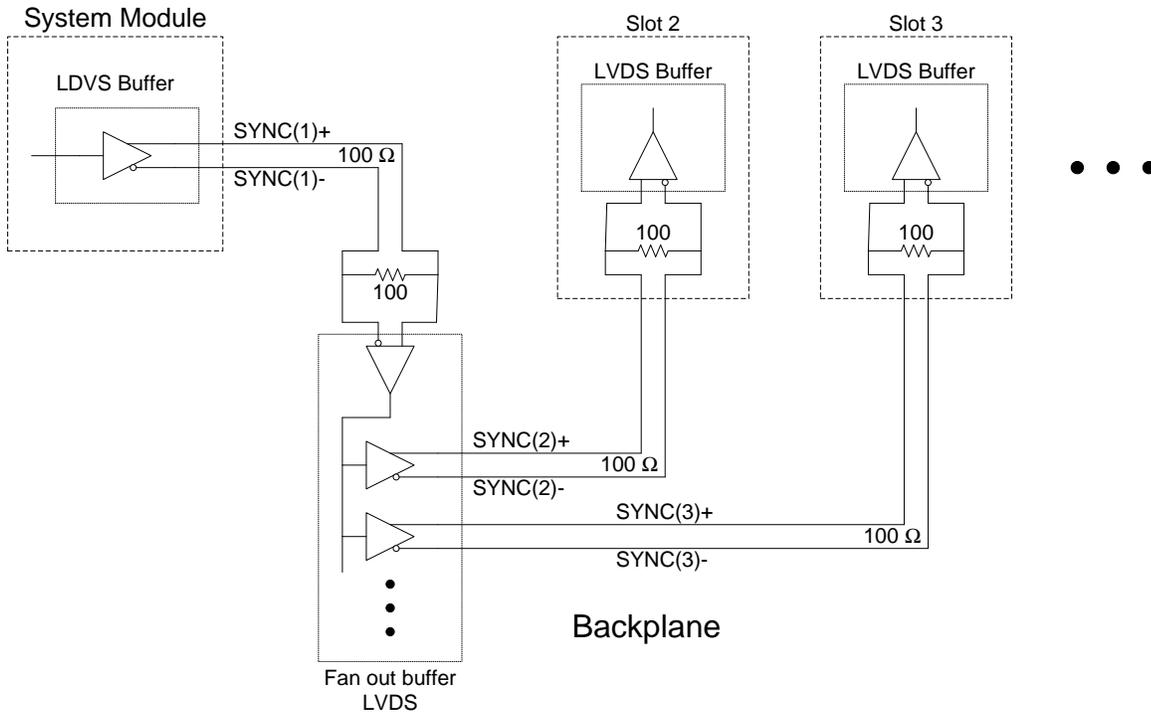
Figure 6-4: Typical SYNC backplane and module implementation.

Compatibility between the system module SYNC output driver and the backplane is enforced by electronic keying. System modules power up with their SYNC drivers disabled. Once the shelf manager has authorized the system module to enable its SYNC output, it is the responsibility of application software to configure the system module's trigger subsystem to drive the SYNC output according to the application's requirements.

RULE 6.51: All SYNC transmitters and receivers SHALL conform to the electrical requirements for LVDS transmitters and receivers.

RULE 6.52: Modules that connect to a SYNC pair SHALL terminate that pair with a 100 Ω ±10% resistor across the signal pair as shown in Figure 6-4.

RULE 6.53: The backplane SHALL terminate the SYNC(1) pair with a 100 Ω ±10% resistor across the signal pair at the input of the LVDS signal distribution buffer as shown in Figure 6-4.

RULE 6.54: AXIe-1 system modules SHALL be able to enable/disable their SYNC drivers.

RULE 6.55: AXIe-1 system module SYNC drivers SHALL default to the disabled state at module power-on, and remain disabled until enabled by the shelf manager.

RECOMMENDATION 6.14: AXIe-1 modules SHOULD treat the SYNC signals as active-high and/or positive-edge triggers, where the "high" is a valid logic state in which SYNC(n)+ is at a more positive voltage than SYNC(n)-.

RECOMMENDATION 6.15: AXIe-1 module functions that make use of received SYNC signals SHOULD have the programmable capability to effectively invert the sense of the received SYNC signal.

The SYNC signal may be driven synchronously to CLK100. The synchronous timing relationship is shown in Figure 6-5. The timing requirements for the system module's SYNC output are shown in Table 6-8. The timing requirements for an instrument module's SYNC input are shown in Table 6-9.

RULE (2.0) 6.3: An AXIe-1 system module SHALL include the programmable capability for the SYNC output to operate either asynchronously or synchronously to CLK100.
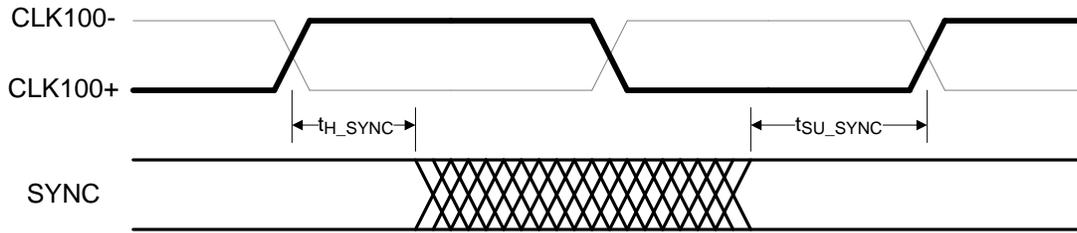
Figure 6-5: Synchronous operation of the SYNC signal.

Parameter	Symbol	Min
SYNC setup time relative to the rising edge of CLK100	t_{SU_SYNC}	3 ns
SYNC hold time relative to the rising edge of CLK100	t_{H_SYNC}	1 ns

Table 6-8 : System module SYNC and CLK100 output timing for synchronous operation.

| Parameter	Symbol	Min
SYNC setup time relative to the rising edge of CLK100	t_{SU_SYNC}	2 ns
SYNC hold time relative to the rising edge of CLK100	t_{H_SYNC}	0 ns

Table 6-9: Instrument module SYNC and CLK100 input timing for synchronous operation.

RULE 6.56: When driving the SYNC signal synchronously to CLK100, a system module's SYNC and CLK100 output signals at the backplane connector SHALL conform to the timing requirements shown in Table 6-8.

RULE 6.57: When sensing the SYNC signal synchronously to CLK100, an instrument module's SYNC and CLK100 inputs at the backplane connector SHALL conform to the timing requirements shown in Table 6-9.

6.6.3 CLK100

The AXIe instrumentation clock resource consists of up to 15 LVDS pairs, CLK100(1:14) and CLK100FB, along with a set of low-skew backplane signal distribution buffers. The signal pair CLK100(1)+/CLK100(1)- connects the system module's LVDS output to the backplane LVDS signal distribution buffers. Each signal pair CLK100(n)+/CLK100(n)- (where $1 < n \leq 14$) connects a buffer output pair to the LVDS input at logical slot *n*. The signal pair CLK100FB+/CLK100FB- (where $1 < n \leq 14$) connects a buffer output pair to the system module's LVDS input. The path delays (including CLK100(1), the backplane buffers, and CLK100(n) and CLK100FB) are matched within 100 ps across all CLK100 paths to provide a low-skew trigger resource to multiple slots. The CLK100 path delays are also matched within 500 ps of each SYNC path. Thus the SYNC signals may operate synchronously with the CLK100 signals. The use of a CLK100 pair by any particular instrument module is entirely application dependent. The backplane electrical design requirements for the instrumentation clock pairs are given in Section 6.1.3, "AXIe Zone 2 Electrical Requirements". The CLK100 topology and connections are illustrated in Figure 6-6.
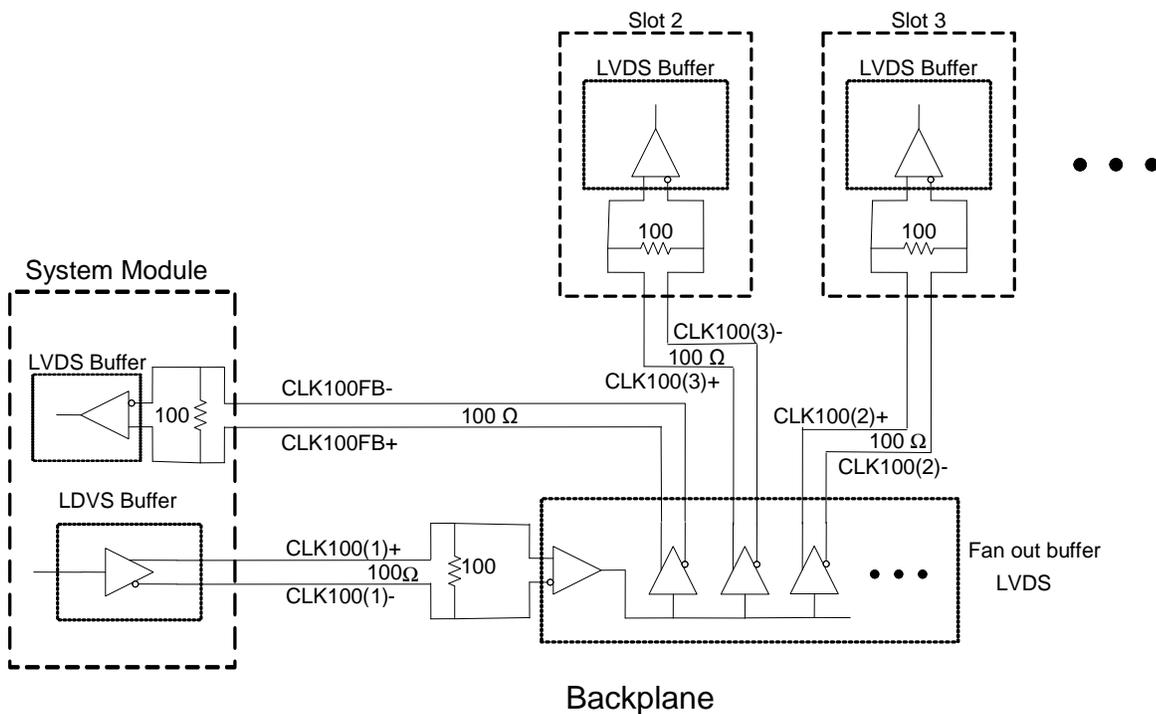
Figure 6-6: Typical CLK100 backplane and module implementation.

Compatibility between the system module's CLK100 output driver and the backplane is enforced by electronic keying. System modules power up with their CLK100 drivers disabled. Once the shelf manager has authorized the system module to enable its CLK100 output, it is the responsibility of application software to configure the system module's trigger subsystem to drive the CLK100 output according to the application's requirements.

RULE 6.58: All CLK100 transmitters and receivers SHALL conform to the electrical requirements for LVDS transmitters and receivers.

RULE 6.59: Modules that connect to a CLK100 pair SHALL terminate that pair with a 100 Ω ±10% resistor across the signal pair as shown in Figure 6-4.

RULE 6.60: The backplane SHALL terminate the CLK100 (1) pair with a 100 Ω ±10% resistor across the signal pair at the input of the LVDS signal distribution buffer as shown in Figure 6-4.

RULE 6.61: AXIe-1 system modules SHALL be able to independently enable/disable their CLK100 drivers.

RULE 6.62: AXIe-1 system module CLK100 drivers SHALL default to the disabled state at module power-on, and remain disabled until enabled by the shelf manager.

PERMISSION 6.12: AXIe-1 system modules MAY have a mechanism for host application software to enable/disable its CLK100 drivers.

RULE 6.63: An AXIe-1 system module's internally-derived CLK100 signal SHALL have a frequency of 100 MHz ±100 ppm and a duty cycle between 45% and 50%.

6.6.4 FCLK

The AXIe fabric clock resource consists of up to 14 pairs, FCLK(1:14), along with a set of low-skew backplane signal distribution buffers. The signal pair FCLK(1)+/FCLK(1)- connects the system module's BLVDS output to the backplane HCSL signal distribution buffers. Each signal pair FCLK(n)+/FCLK(n)- (where $1 < n \leq 14$) connects a buffer output pair to the HCSL input at logical slot n. The FCLK signal is the reference clock for all of the fabric PCI Express ports. All modules that have fabric PCI Express ports are required to use FCLK as the reference clock for

those ports. The 100 MHz clock may be either constant frequency or spread spectrum and must comply with the PCI Express reference clock specifications. The backplane electrical design requirements for the fabric clock pairs are given in Section 6.1.3, "AXIe Zone 2 Electrical Requirements". The FCLK topology and connections are illustrated in Figure 6-7.
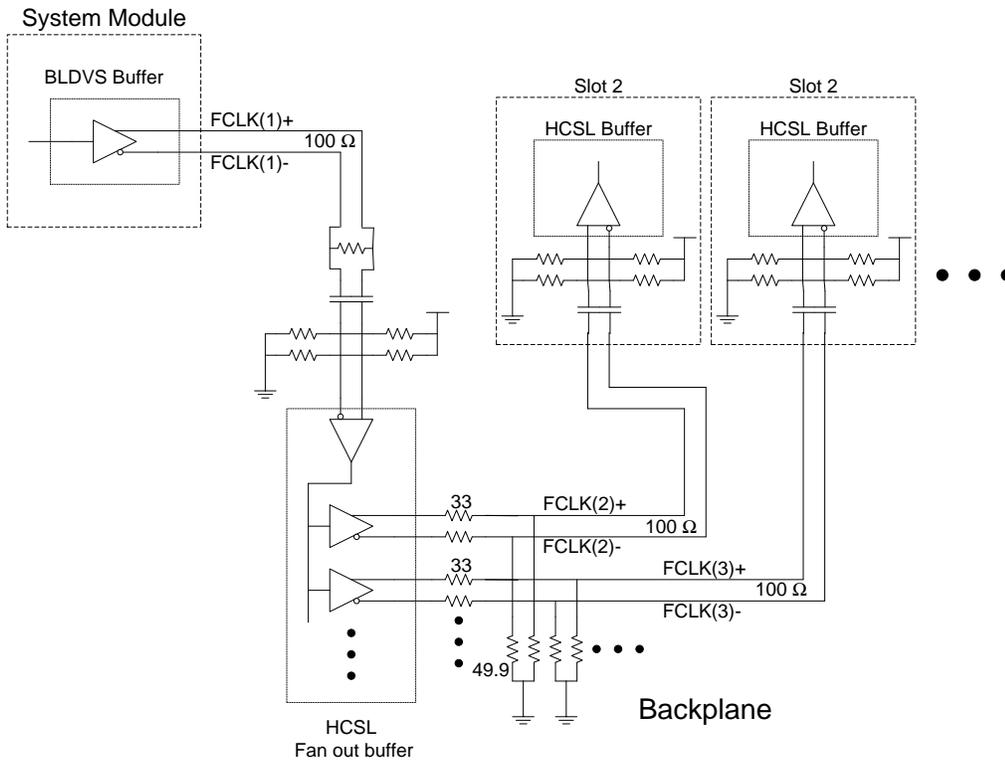
Figure 6-7: Typical backplane and module FCLK implementation.

Compatibility between the system module's FCLK output driver and the backplane is enforced by electronic keying. System modules power up with their FCLK drivers disabled. Once the shelf manager has authorized the system module to enable its FCLK output, the system module begins driving its FCLK output with the 100 MHz PCIe reference clock.

RULE 6.64: AXIe FCLK clock generators, backplane FCLK transmitters, and module FCLK receivers SHALL conform to the electrical requirements for PCI Express reference clocks as defined in the PCI Express® Base Specification and the PCI Express® Card Electromechanical Specification.

RULE 6.65: A system module's FCLK output driver SHALL conform to the electrical requirements for BLVDS drivers.

RULE 6.66: An AXIe-1 backplane's FCLK receiver SHALL be compatible with BLVDS signal levels and tolerant of MLVDS signal levels.

RULE 6.67: An AXIe-1 instrument module's FCLK receiver SHALL be tolerant of BLVDS and MLVDS signal levels.

RULE 6.68: The backplane SHALL terminate the FCLK(1) pair with a 100 Ω ±10% resistor across the signal pair at the input of the LVDS signal distribution buffer as shown in Figure 6-7.

PERMISSION 6.13: The backplane and module FCLK receivers MAY have capacitive isolation and bias networks as shown in Figure 6-7 to achieve a wide common-mode input signal tolerance.

RULE 6.69: AXIe-1 system modules SHALL be able to independently enable/disable their FCLK drivers.

RULE 6.70: AXIe-1 system module FCLK drivers SHALL default to the disabled state at module power-on, and remain disabled until enabled by the shelf manager.

PERMISSION 6.14: AXIe-1 system modules MAY have a mechanism for host application software to enable/disable their FCLK drivers.

6.7 AXIe Trigger Bus Requirements

The AXIe trigger bus is a set of 12 MLVDS trigger lines, TRIG(0:11), that are bused across, and connected to, all of the AXIe-1 backplane slots. The topology and driver/receiver electrical requirements are similar to those for the AdvancedTCA® synchronization clock interface. The use of the AXIe trigger lines by any particular module is entirely application dependent. Figure 6-8 illustrates the backplane implementation of and module connections to one of the TRIG pairs.
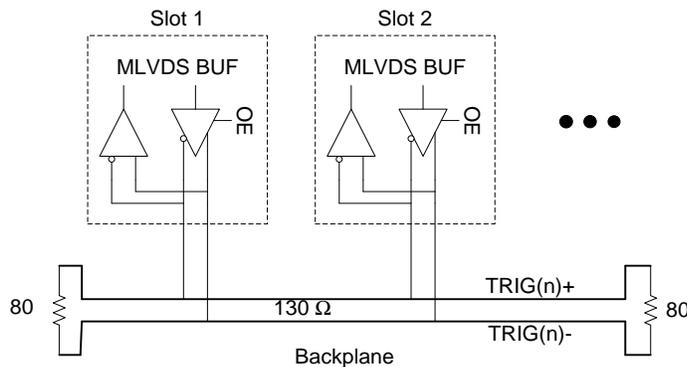
Figure 6-8: Typical AXIe trigger bus implementation.

The backplane electrical design requirements for the AXIe trigger bus are given in Section 6.1.3, "AXIe Zone 2 Electrical Requirements".

There are no electronic keying requirements for the AXIe trigger bus. Modules power up with their trigger bus drivers disabled. It is the responsibility of application software to determine which modules are permitted to drive any particular TRIG pair at a given time.

The AXIe trigger bus utilizes MLVDS drivers and receivers. The receivers are Type 2 MLVDS, which has a 100 mV input threshold offset, and presents a stable output in the absence of a differential input signal.

RULE (2.0) 6.4: All TRIG transmitters SHALL conform to the electrical requirements for MLVDS transmitters and receivers.

RULE (2.0) 6.5: All TRIG receivers SHALL conform to the electrical requirements for Type 2 MLVDS receivers.

RULE 6.71: AXIe-1 modules SHALL NOT drive any of the TRIG(0:11) lines unless they have been explicitly enabled by host application software.

RULE 6.72: AXIE trigger bus ports SHALL conform to the AdvancedTCA® requirements 6.120-6.124 for Synchronization Clock ports.

6.8 AXIe Local Bus

The AXIe local bus consists of 18, 42, or 62 differential pairs providing point-to-point connections between adjacent instrument slots. In the case of a backplane whose system slot is not physical slot 1, a local bus segment connects the two instrument slots that are adjacent to, and on each side of, the system slot. All AXIe-1 backplanes provide at least 18 local bus pairs in each segment and may optionally provide 42 or 62 pairs.

This specification does not define any local bus protocols. Instead, local bus connections will typically be between two modules from a single vendor utilizing a proprietary protocol. Compatibility is enforced by electronic keying. See Section 3.1.9, "AXIe Local Bus Electronic Keying".

The backplane electrical design requirements for the local bus are given in Section 6.1.3,"AXIe Zone 2 Routing Requirements".

The AXIe local bus is similar in nature to the AdvancedTCA® Update Channel interface. They have many of the same design requirements.

Axie modules are permitted to drive the local bus pins with up to 1.6 Volts, regardless of E-keying. Higher voltage signals (up to 2.5V) must strictly observe E-keying. Signal voltages greater than 2.5 Volts are not permitted on the Local Bus.

RULE 6.73 AXIe local bus ports SHALL conform to the AdvancedTCA® requirements 6.125-6.128 for Update Channel ports.

RULE 6.74 AXIe local bus channels SHALL be enabled and disabled as single-port channels of either 18, 42, or 62 pairs.

RULE 6.75: From power-on until it is explicitly enabled by the shelf manager, a Local Bus Pin SHALL present to the backplane:

- **Open-circuit voltage in the 0 V to 1.6 Volt range, relative to logic ground.**
- **Source/load resistance of 50 Ω or greater.**

RULE 6.76: AXIe local bus drivers SHALL operate within the 0 Volt to +2.5 Volt range, relative to logic ground.

RULE 6.77: [deleted]

RULE 6.78:   [deleted]

7. Electromagnetic Compatibility (EMC)

The AXIe-1 architecture is designed to support a variety of general-purpose instrumentation, including very sensitive signal generation and measurement modules. To help assure that these modules can operate within their published specifications, the AXIe-1 architecture includes various recommendations for the electromagnetic emissions and susceptibility of AXIe-1 modules and mainframe components. These recommendations cover both conducted EMC on the power distribution conductors and radiated EMC between the modules.

7.1 Conducted EMC

7.1.1 Chassis and Power Supply Conducted Emissions and Susceptibility

Chassis power supplies are characterized by their **Peak Current (I_P)** and their **Dynamic Current (I_D).** The chassis peak current is the power supply's rated maximum dc output current. The chassis dynamic current is a measure of its capacity to power dynamic loads in the 20 Hz to 1 GHz frequency range.

RECOMMENDATION 7.1: An AXIe-1 chassis -48V power supply SHOULD tolerate 0-20 Hz load variations from 0A to the power supply's rated peak current without generating voltage variations in excess of 1.00 V peak-to-peak in the 0-20 Hz range.

RECOMMENDATION 7.2: An AXIe-1 chassis -48V power supply SHOULD tolerate the dynamic peak-to-peak loading specified in Figure 7-1 without generating total peak-to-peak voltage variations in excess of the limits shown in Figure 7-2.
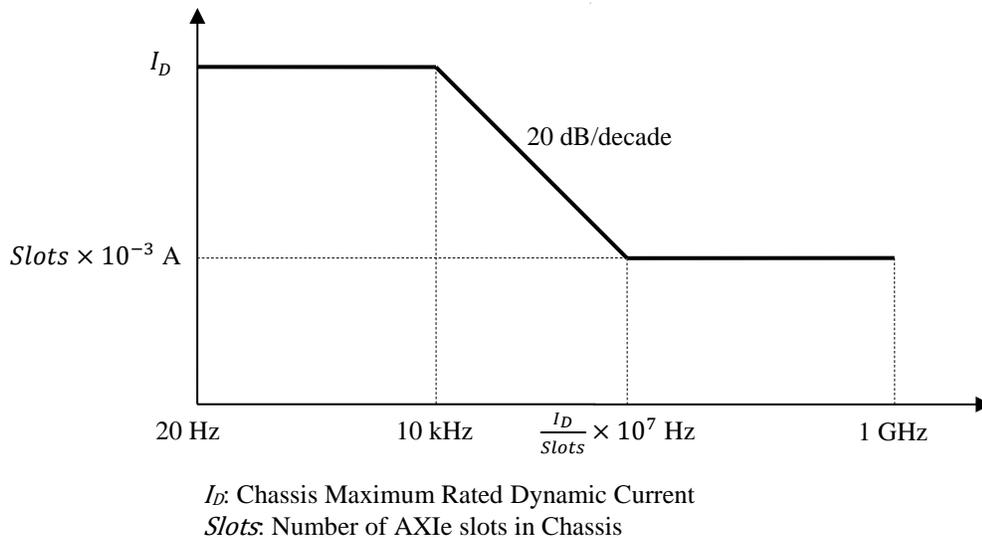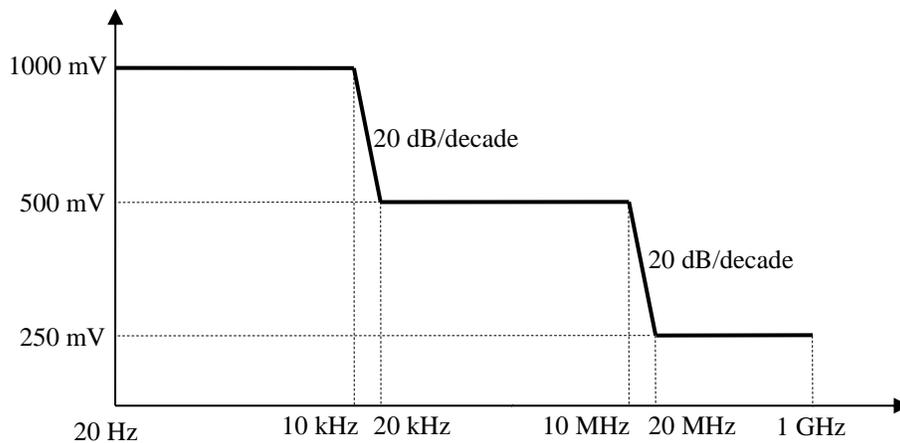

I_D: Chassis Maximum Rated Dynamic Current
Slots: Number of AXIe slots in Chassis

Figure 7-1: Chassis Load Current.

Figure 7-2: Chassis total induced noise and ripple.

7.1.2 Module Conducted Emissions

AXIe-1 modules are characterized by their **Peak Current (I_{Pm})** and their **Dynamic Current (I_{Dm}).** The module peak current is the module's maximum rated instantaneous current in the dc to 10 MHz range, drawn from the backplane supply. The module dynamic current is a measure of the module's worst-case power supply current variation in the 20 Hz to 1 GHz frequency range.

RECOMMENDATION 7.3: A module's specifications SHOULD include a peak current rating such that the module's instantaneous current draw from the -48V supply does not exceed that peak current rating.

RECOMMENDATION 7.4: A module's specifications SHOULD include a dynamic current rating that the characterizes that module's conducted emissions in accordance with Figure 7-3. The module's conducted emissions on the -48V power supply SHOULD NOT exceed the levels shown in Figure 7-3.

I_{Dm}: Module Maximum Rated Dynamic Current
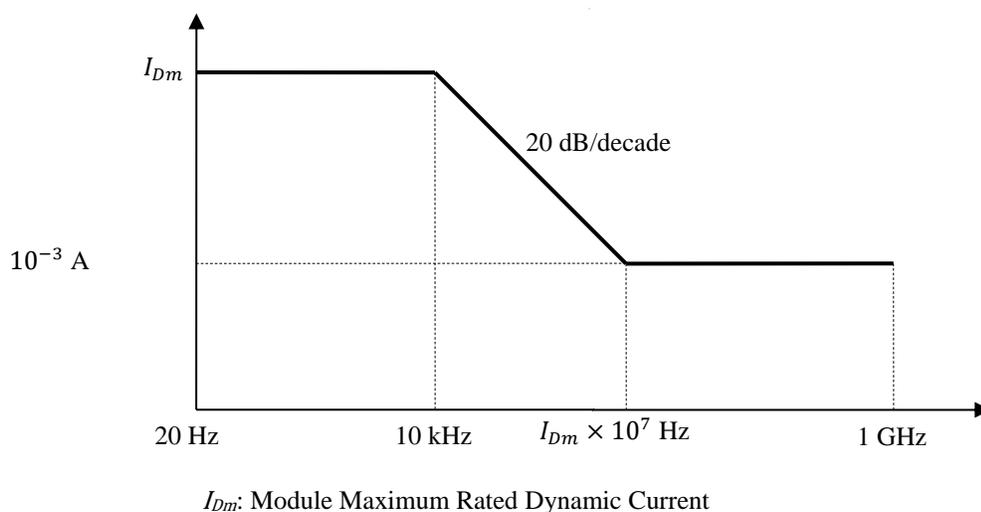
Figure 7-3: Module Conducted Emissions.
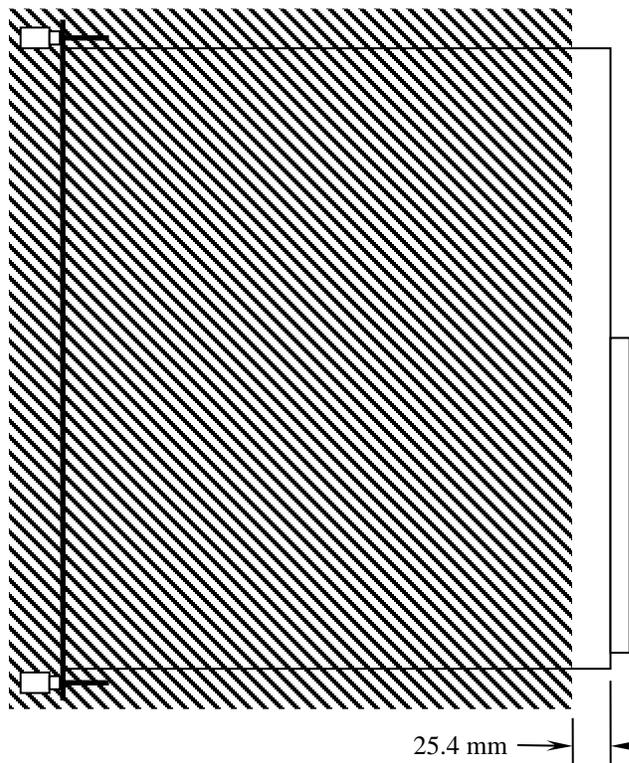
7.1.3 Module Conducted Susceptibility

RECOMMENDATION 7.5: Each module SHOULD operate within its published specifications in the presence of the backplane power supply noise levels shown in Figure 7-2.
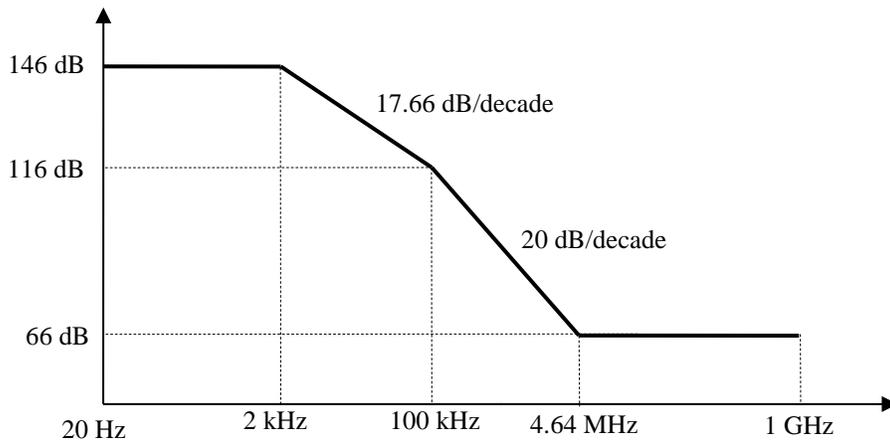
7.2 Radiated EMC

7.2.1 Radiated Emissions

RECOMMENDATION 7.6: The close-field magnetic emissions measured at the pitch line on either side of a module in the shaded area shown in Figure 7-4 SHOULD NOT exceed the limits shown in Figure 7-5.


25.4 mm →

Figure 7-4: Module radiated emissions test area.

Figure 7-5: Module close field radiated emissions limit (dB above 1 picoTesla).

7.2.2 Radiated Susceptibility

RECOMMENDATION 7.7: Each AXIe-1 module SHOULD operate within its published specifications in the presence of the magnetic field levels shown in Figure 7-6 on either side of the module at the pitch line in the shaded regions of Figure 7-7.
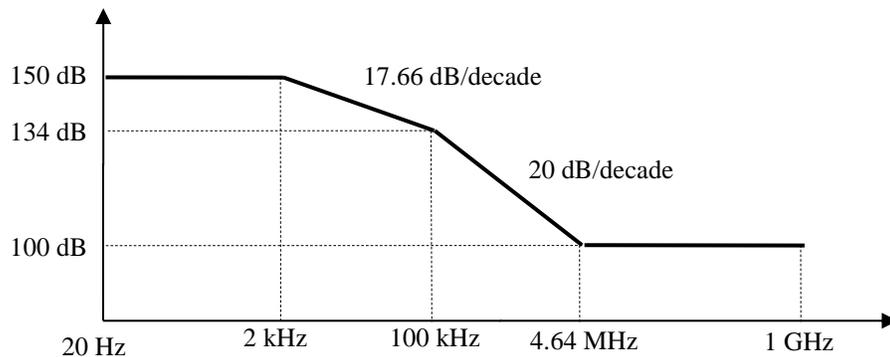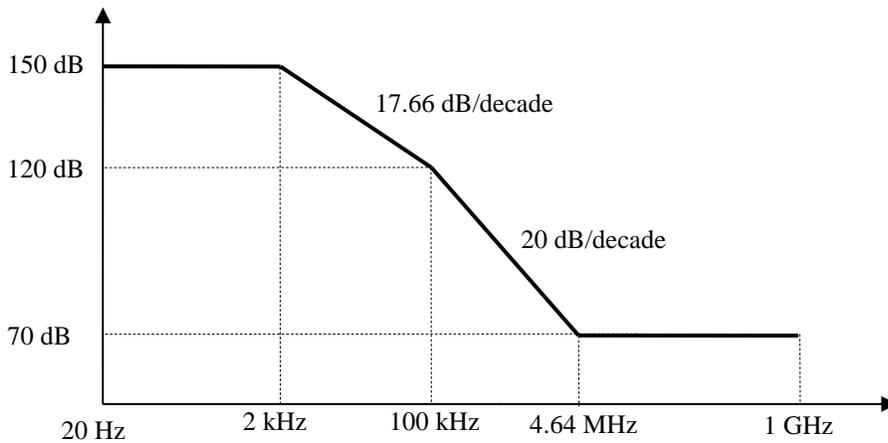

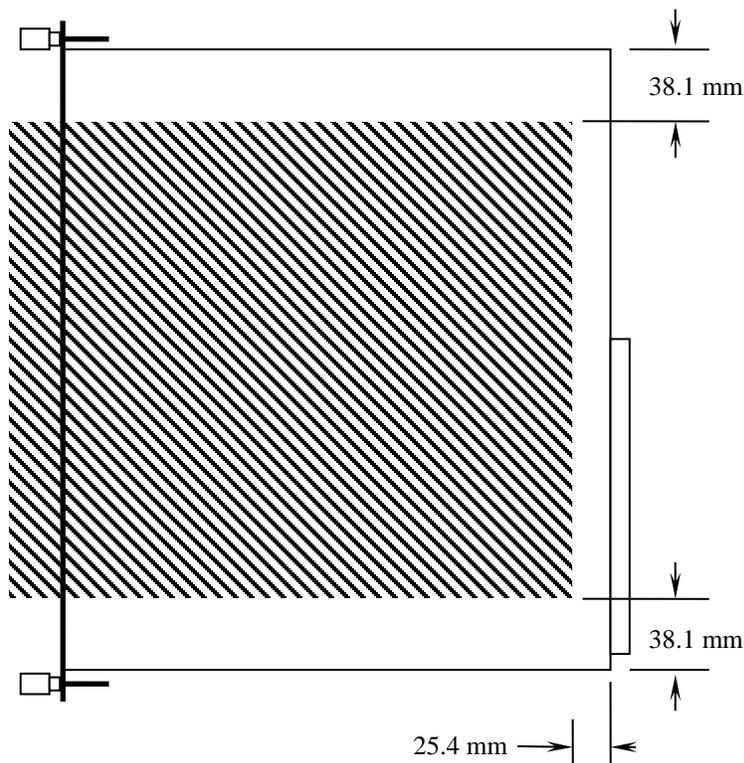**Figure 7-6: Module radiated susceptibility limits near top and bottom edges (dB above 1 picoTesla).**
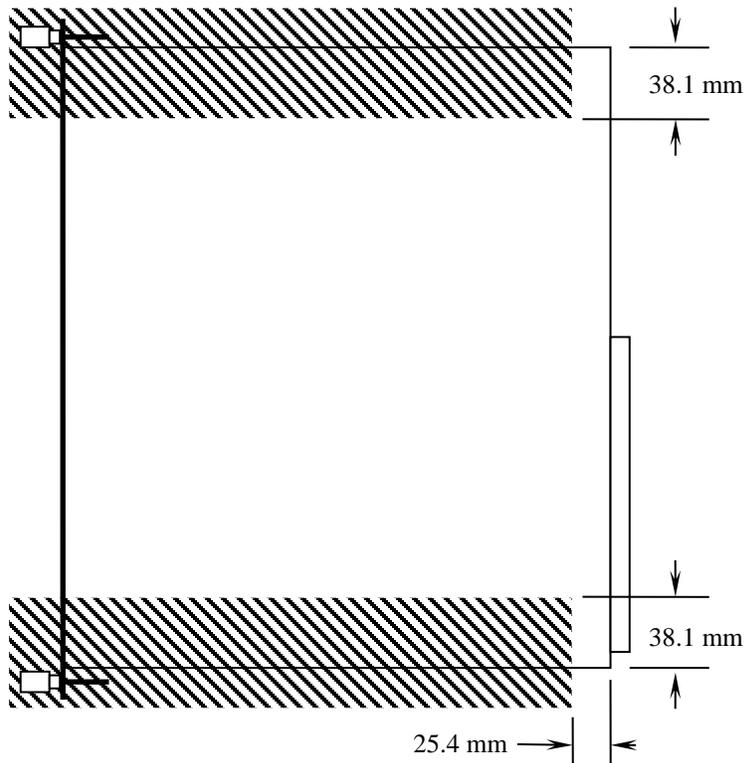
Figure 7-7: Module edge radiated susceptibility test area.

RECOMMENDATION 7.8: Each AXIe-1 module SHOULD operate within its published specifications in the presence of the magnetic field levels shown in Figure 7-8 on either side of the module at the pitch line in the shaded regions of Figure 7-9.

Figure 7-8: Module radiated susceptibility limits (dB above 1 picoTesla).

Figure 7-9: Module center radiated susceptibility test area.

7.2.3 Regulatory Compliance

Each AXIe-1 module's manufacturer is responsible to determine and specify which regulatory radiated EMC requirements that the module meets. The actual emissions from that module must be only a fraction of the total emissions permitted by the regulatory agency in order that a fully-loaded 14-slot chassis will meet the specified emissions level.

RECOMMENDATION 7.9: An AXIe-1 module's manufacturer SHOULD specify the conditions necessary for a mainframe containing that module to meet the specified regulatory emission limits.

RECOMMENDATION 7.10: Module manufacturers SHOULD perform regulatory emissions testing of individual modules to levels significantly below the regulatory agency specified levels in order to accommodate the inclusion of multiple modules within an AXIe-1 chassis.

7.3 EMC Test Methods

The AXIe-1 specifications for electromagnetic compatibility are based heavily on the VXIbus EMC specifications. The VXIbus specification includes suggested EMC test methods. Those test methods should be generally applicable to AXIe EMC testing as well.

RECOMMENDATION 7.11: AXIe manufacturers SHOULD use EMC test methods similar to those described in Section B.8.7, "Suggested Test Methods" of the VMEbus Extensions for Instrumentation System Specification.